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(71) Applicant: **Ohmi, Tadahiro**
Sendai-shi, Miyagi-ken 980-0813 (JP)

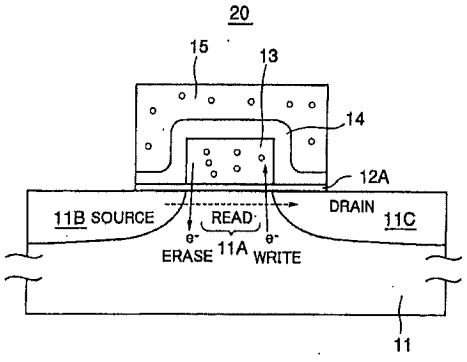
(72) Inventors:
- **OHMI, Tadahiro**
Sendai-Shi, Miyagi 980-0813 (JP)
- **SUGAWA, Shigetoshi; c/o DEP. ELEC. ENG. 05, Aza-Aoba, Aramaki, Aoba-K (JP)**
- **HIRAYAMA, Masaki; c/o DEP. ELEC. ENG. 05, Aza-Aoba, Aramaki, Aoba-K (JP)**
- **SHIRAI, Yasuyuki; c/o DEP. ELEC. ENG. 05, Aza-Aoba, Aramaki, Aoba-K (JP)**

(74) Representative: **Liesegang, Roland, Dr.-Ing.**
FORRESTER & BOEHMERT
Pettenkoferstrasse 20-22
80336 München (DE)

(54) DIELECTRIC FILM AND METHOD OF FORMING IT, SEMICONDUCTOR DEVICE, NONVOLATILE SEMICONDUCTOR MEMORY DEVICE, AND PRODUCTION METHOD FOR SEMICONDUCTOR DEVICE

(57) In a film formation method of a semiconductor device including a plurality of silicon-based transistors or capacitors, there exist hydrogen at least in a part of the silicon surface in advance, and the film formation method removes the hydrogen by exposing the silicon surface to a first inert gas plasma. Thereafter a silicon compound,layer is formed on the surface of the silicon gas by generating plasma while using a mixed gas of a second inert gas and one or more gaseous molecules, such that there is formed a silicon compound layer containing at least a pat of the elements constituting the gaseous molecules, on the surface of the silicon gas.

FIG.23



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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device in which an oxide film, a nitride film, an oxynitride film, and the like, is formed on a silicon semiconductor, and the formation method thereof.

BACKGROUND ART

[0002] The gate insulation film of a MIS (metal/insulator/silicon) transistor is required to have various high-performance electric properties and also high reliability, such as low leakage current characteristic, low interface state density, high breakdown voltage, high resistance against hot carriers, uniform threshold voltage characteristic, and the like.

[0003] In order to satisfy these various requirements, the technology of thermal oxidation process has been used conventionally as the formation technology of the gate insulation film, wherein the thermal oxidation technology uses oxygen molecules or water molecules at the temperature of about 800°C or more.

[0004] It should be noted that a thermal oxidation process has been conducted conventionally after conducting a preprocessing process of removing surface contaminants such as organic materials, metals, particles, and the like, by a conducting cleaning process. It should be noted that such a conventional cleaning process includes a final cleaning process that uses a diluted hydrofluoric acid or hydrogenated water for terminating the dangling bonds exiting on the silicon surface by hydrogen. Thereby, formation of native oxide film on the silicon surface is suppressed, and the silicon substrate thus having a cleaned surface is forwarded to the following process of thermal oxidation. In the thermal oxidation process, the terminating hydrogen at the surface undergoes decoupling during the process of raising the temperature of the silicon substrate in an inert gas atmosphere such as argon (Ar) gas atmosphere. Oxidation of the silicon surface is conducted thereafter at the temperature of about 800°C or more in the atmosphere in which oxygen molecules or water molecules are introduced.

[0005] In the conventional thermal oxidation process, satisfactory oxide/silicon interface characteristics, oxide breakdown characteristics, leakage current characteristics, and the like, are achieved only in the case a silicon surface having the (100) orientation is used for the formation of the silicon oxide film. Further, it is known that there arises a remarkable deterioration of leakage characteristic in the case the thickness of the silicon oxide film thus formed by the conventional thermal oxidation process is reduced to about 2nm or less. Thus, it has been difficult to realize a high-performance miniaturized transistor that requires decrease of the gate insulation film thickness.

[0006] Further, in the case the silicon oxide film is formed on a silicon crystal having a surface orientation other than the (100) orientation or on a polysilicon formed on an insulation film, there arises a problem of formation of large interface state density at the oxide/silicon interface as compared with the case the silicon oxide film is formed on the (100)-oriented silicon surface, and this holds true even when the silicon oxide film is formed by the thermal oxidation technology. It should be noted that a polysilicon film formed on an insulation film has a primarily (111) oriented surface. Thus, such a silicon oxide film has poor electric properties in terms of breakdown characteristics, leakage current characteristics, and the like, particularly when the thickness thereof is reduced, and there has been a need of increasing the film thickness of the silicon oxide film when using such a silicon oxide film.

[0007] Meanwhile, the use of large-diameter silicon wafer substrate or large-area glass substrate is increasing these days for improving the efficiency of semiconductor device production. In order to form transistors on the entire surface of such a large-size substrate with uniform characteristics and with high throughput, it is necessary to form the insulation film at a low temperature so as to decrease the magnitude of the temperature change, which takes place at the time of the heating process or at the time of the cooling process. Further, the process of forming such an insulation film is required to have small temperature dependence. In the, conventional thermal oxidation process, it should be noted that there has been a large fluctuation of oxidation reaction rate caused by temperature fluctuation, and it has been difficult to conduct the production process of semiconductor devices with high throughput while using a large-area substrate.

[0008] In order to solve these problems associated with the conventional thermal oxidation technology, various low-temperature film formation processes have been attempted. Among others, the technology disclosed in Japanese Laid-Open Patent Publication 11-279773 or the technology disclosed in Technical Digest of International Electron Devices Meeting, 1999, pp.249-252, or in 2000 Symposium on VLSI Technology Digest of Technical Papers, pp.76-177, achieves relatively good electronic properties for the film by conducting the oxidation of the silicon surface by using atomic state oxygen O*. There, an inert gas having a large metastable level is used for the atomization of the oxygen molecules, and for this, the inert gas is introduced into plasma together with gaseous oxygen molecules.

[0009] In these technologies, it should be noted that a microwave is irradiated to the mixed gas formed of an inert krypton (Kr) gas and an oxygen (O_2) gas, and a large amount of atomic state oxygen O* are formed. Thereby, the oxidation of silicon is conducted at a temperature of about 400°C, and the properties comparable to those of the conventional thermal oxidation process, such as low leakage current characteristics, low inter-

face state density high breakdown voltage, and the like, are achieved. Further, according to this oxidation technology, a high-quality oxide film is obtained also on the silicon surface having a surface orientation other than the (100) surface.

[0010] On the other hand, such a conventional silicon oxide film formation technology, even when using the microwave plasma, could at best realize a silicon oxide film having electric properties comparable to those of the film formed by the conventional thermal oxidation process, which uses oxygen molecules or water molecules. Particularly, it has been not possible to obtain the desired low leakage current characteristics in the case the silicon oxide film has a thickness of about 2nm or less on the silicon substrate surface. Thus, it has been difficult to realize high-performance, miniaturized transistors that require further decrease of the gate insulation film thickness, similarly to the case of conventional thermal oxide film formation technology.

[0011] Further, there has been a problem that the silicon oxide film thus formed shows severe degradation of electric properties in the case the silicon oxide film is used for a transistor, such as degradation of conductance caused by hot carrier injection or increase of leakage current in the case the silicon oxide film is used in a device such as a flash memory, which relies upon tunneling of electrons caused through the silicon oxide film, as compared with the case of using a silicon oxide film formed by the conventional thermal processes.

[0012] FIG. 1 shows the schematic structure of a conventional flash memory device 10.

[0013] Referring to FIG. 1, the flash memory device 10 is formed on a silicon substrate 11 doped to p-type or n-type and there is formed a floating gate electrode 13 on the silicon substrate 11 via a tunneling oxide film 12. The floating gate electrode 13 is covered with an inter-electrode insulation film 14, and a control gate electrode 15 is formed on the floating gate electrode 13 via the inter-electrode insulation film 14. Further, a source region 11B and a drain region 11C of n-type or p-type are formed in the silicon substrate 11 at both lateral sides of a channel region 11A right underneath the floating gate electrode 13.

[0014] In the flash memory device 10 of FIG. 1, the control gate electrode 15 causes capacitance coupling with the floating gate electrode via the inter-electrode insulation film 14, and as a result, the potential of the floating gate electrode is controlled by the control voltage applied to the control gate electrode 15.

[0015] Thus, in the case information is written into the floating gate electrode in the flash memory device 10 of FIG. 1, a predetermined drive voltage is applied across the drain region 11C and the source region 11B and a predetermined positive write voltage is applied to the control gate electrode 15. Thereby, there are formed hot electrons as a result of acceleration in the vicinity of the drain region 11C, and the hot electrons thus formed are injected into the floating gate electrode 13 via the tunneling oxide film 12.

[0016] In the case the information thus written is to be erased, a predetermined erase voltage is applied to the silicon substrate 11 or to the source region 11B, and the electrons in the floating gate electrode 13 are pulled out. In the case of reading the written information, a predetermined read voltage is applied to the control gate electrode 15 and the electron current flowing through the channel region 11A from the source region 11B to the drain region 11C is detected.

[0017] FIG.2A shows the band structure of the flash memory 10 of FIG. 1 in the cross-sectional view that includes the floating gate electrode 13, the tunneling oxide film 12 and the silicon substrate 11, wherein FIG. 2A shows the state in which no control voltage is applied to the control gate electrode 15.

[0018] Referring to FIG.2A, the tunneling insulation film 12 forms a potential barrier and it can be seen that the injection of the electrons on the conduction band Ec of the silicon substrate 11 into the floating gate electrode 13 is effectively blocked.

[0019] FIG.2B shows the band structure for the case a write voltage is applied to the control gate electrode 15.

[0020] Referring to FIG.2B, there is induced modification of the band structure in the tunneling insulation film 12 as a result of application of the write voltage, and as a result, the conduction band Ec forms a triangular potential. Thus, the hot electrons thus formed in the channel region A are injected into the floating gate electrode 13 after passing through the triangular potential barrier in the form of Fowler-Nordheim tunneling current.

[0021] Now, in order to increase the writing speed in the flash memory device 10, there is a need of increasing the tunneling probability of the tunneling current passing through the triangular potential in the state of FIG. 2B. This can be achieved by decreasing the thickness of the tunneling oxide film 12. In the case the thickness of the tunneling oxide film 12 is decreased, on the other hand, the electrons in the channel may pass through the tunneling oxide film 12 in the non-writing state shown in FIG.2B by causing tunneling and form a leakage current.

[0022] FIG.3 shows the relationship between the electric field applied to the tunneling oxide film 12 and the current density of the tunneling current passing through the tunneling oxide film 12.

[0023] Referring to FIG.3, it is required that a tunneling current of about $1A/cm^2$ can flow through the tunneling oxide film 12 in response to an electric field of about 10MV/cm applied to the tunneling oxide film 12 in the writing state of FIG. 2B when to realize the writing time of 1 - 10μ seconds in the flash memory device 10. In the case of non-writing state of FIG.2A, on the other hand, it is required that the leakage current through the tunneling oxide film 12 be suppressed to $10^{-15}A/cm^2$ or less at the application electric filed of $1MV/cm^2$. Thus, the conventional flash memory device 10 realizes the

electric field - current characteristic shown in FIG.3 by a straight line by using a thermal oxides film having a thickness of several nanometers for the tunneling oxide film 12.

[0024] On the other hand, when an attempt is made to reduce the thickness of the tunneling oxide film 12 for reducing the write time, the electric field-current characteristic of the tunneling oxide film 12 is changed as represented in FIG.3 by a curved line. There, it can be seen that, while there is caused a large increase of the tunneling current in the case the electric field of 10MV/cm is applied, and while the conventional tunneling current density of 1A/cm^2 is realized in the state of low electric field, there is caused a large increase in the leakage current in the non-writing state, and thus, the information written into the floating gate electrode 13 is no longer retained.

DISCLOSURE OF THE INVENTION

[0025] Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor device and fabrication process thereof wherein the foregoing problems are eliminated.

[0026] Another object of the present invention is to provide a dielectric film showing a small leakage current and is capable of providing a tunneling current of large current density at the time of application of an electric field, as well as a formation method thereof.

[0027] Another object of the present invention is to provide a semiconductor device or a non-volatile semiconductor device that uses such a dielectric film and a fabrication method of such a semiconductor device.

[0028] Another object of the present invention is to provide a dielectric film formed on a silicon surface,

said dielectric film containing nitrogen with a concentration distribution such that a nitrogen concentration increases at a dielectric film surface as compared to a central part of the dielectric film.

[0029] Another object of the present invention is to provide a semiconductor device, comprising:

a silicon substrate;
an insulation film formed on said silicon substrate; and
an electrode formed on said insulation film,

wherein said insulation film has a nitrogen concentration distribution such that a nitrogen concentration increases at a film surface contacting with said electrode as compared with a central part of said film.

[0030] Another object of the present invention is to provide a non-volatile semiconductor memory device, comprising:

a silicon substrate;
a tunneling insulation film formed on said silicon substrate;
a floating gate electrode formed on said tunneling insulation film; and
a control gate electrode formed on said floating gate electrode via an inter-electrode insulation film,
one of said insulation films having a nitrogen concentration distribution such that a nitrogen concentration increases at the film surface contacting with said electrode as compared with a central part of said film.

[0031] Another object of the present invention is to provide a method of forming a dielectric film, comprising the steps of:

forming a silicon oxide film on a surface;
modifying a surface of said silicon oxide film by exposing the same to hydrogen nitride radicals NH*.

[0032] Another object of the present invention is to provide a method of forming a dielectric film, comprising the steps of:

forming a silicon oxide film on a surface; and
modifying a surface of said silicon oxide film by exposing the same to microwave plasma formed in a mixed gas of an inert gas selected from Ar or Kr and a gas containing nitrogen and hydrogen as constituent elements.

[0033] Another object of the present invention is to provide a method of forming a dielectric film comprising the step of exposing a silicon surface to microwave plasma formed in a mixed gas of an inert gas primarily formed of Kr, a gas containing nitrogen as a constituent element and a gas containing oxygen as a constituent element, to form an oxynitride film on said silicon surface.

[0034] Another object of the present invention is to provide a method of fabricating a semiconductor device, comprising the steps of;

forming a silicon oxide film on a silicon substrate by an oxidation processing;
modifying a surface of said silicon oxide film by exposing the same to hydrogen nitride radicals NH*; and
forming a gate electrode on said modified silicon oxide film.

[0035] Another object of the present invention is to provide a method of fabricating a semiconductor device, comprising the steps of:

forming a silicon oxide film on a silicon substrate by an oxidation processing;
modifying a surface of said silicon oxide film by exposing the same to microwave plasma formed in a mixed gas of an inert gas selected from Ar or Kr and

a gas containing nitrogen and hydrogen as constituent elements; and
forming a gate electrode on said modified silicon oxide film.

[0036] Another object of the present invention is to provide a fabrication method of a semiconductor device, comprising the steps of:

exposing a silicon substrate surface to microwave plasma formed in a mixed gas of an inert gas primarily formed of Kr, a gas containing nitrogen as a constituent element and a gas containing oxygen as a constituent element, to form an oxynitride film on said silicon surface; and
forming a gate electrode on said oxynitride film.

[0037] According to the present invention, the surface of the oxide film is modified by exposing the surface of the oxide film formed on a surface of a silicon substrate or the like to microwave plasma formed in a mixed gas of an inert gas primarily formed of Ar or Kr and a gas containing nitrogen and hydrogen, and nitrogen are concentrated to a surface region of the oxide film within the depth of several nanometers. Nitrogen thus concentrated to the oxide film surface form a substantially layered nitride region on the oxide film surface, and as a result, the oxide film is changed to a structure approximately similar to the one in which a nitride film is laminated on the surface of the silicon oxide film.

[0038] In the dielectric film having such a structure, there is provided a region of small bandgap in correspondence to the nitride region adjacent to a region of large bandgap corresponding to the silicon oxide film region, and because of the fact that the nitride region has a specific dielectric constant larger than that of the silicon oxide film, the dielectric film structure shows an effectively large film thickness with regard to the electrons in the channel region 11A in the state that no control voltage is applied to the control gate electrode 15, and the tunneling of the electrons is effectively blocked.

[0039] In the case a write voltage is applied to the control gate electrode 15, on the other hand, the band structures of the oxide film region and the nitride region constituting the dielectric film structure are changed. Thereby, the effective thickness of eth oxide film region is reduced with the formation of the nitride region, and as a result, the hot electrons in the channel region 11A are' allowed to cause tunneling through the dielectric film structure efficiently. Because the nitride region formed on the surface of the oxide film region has a small bandgap, it does not function as a potential barrier to the hot electrons to be injected.

[0040] As a result of using such a dielectric film structure for the tunneling insulation film of the non-volatile semiconductor memory device such as a flash memory, and the like, it becomes possible to increase the wiring speed or reduce the operational voltage while simultaneously reducing the leakage current.

[0041] It should be noted that such an oxide film, in which there is caused nitrogen concentration at the surface part thereof, can be formed also by exposing the silicon surface to microwave plasma formed in a mixed gas of an inert gas primarily formed of Kr, a gas containing nitrogen as a constituent element and a gas containing oxygen as a constituent element. The oxide film thus formed has the composition of an oxynitride film as a whole, while it should be noted that a part of nitrogen are concentrated in such a structure to the interface between the oxynitride film and the silicon surface for relaxing the stress, while other nitrogen are concentrated to the film surface and form the desired nitride layer region. In the oxynitride film of such a structure, there is caused stress relaxation by the nitrogen concentrated to the interface to the silicon substrate, and because of this, the density of the electric charges trapped in the film or the density of the interface states is reduced and the leakage current path other than the tunneling mechanism is effectively blocked. Thus, the oxynitride film obtained according to such a process has an extremely high film quality. In such an oxynitride film, it is preferable that the hydrogen concentration contained in the film is $10^{12}cm^{-2}$ or less, preferably $10^{11}cm^{-2}$ or less in terms of surface density.

[0042] As the formation of the dielectric film can be conducted at a low temperature of 550°C or less in the present invention, it is possible to recover the oxygen defects in the film without decoupling the hydrogen terminating the dangling bonds in the oxide film. This applied also to the formation of the nitride film or oxynitride film to be explained later.

BRIEF DESCRIPTION OF THE DRAWINGS

[0043]

FIG. 1 is a diagram showing the construction of a conventional flash memory device;
FIGS.2A and 2B are diagrams explaining the operation of the flash memory device;
FIG.3 is a diagram explaining the problems of the conventional flash memory device;
FIGS.4A - 4C are diagrams showing the formation process of an oxide film and the fabrication process of a semiconductor device according to a first embodiment of the present invention;
FIG.5 is a diagram showing the schematic construction of a plasma apparatus having a radial line slot antenna and used in the present invention;
FIG.6 is a characteristic diagram showing the exposure effect of the bond formed between the surface-terminating hydrogen at the silicon surface and silicon caused by exposure to Kr plasma as obtained by infrared spectroscopy;
FIG.7 is a characteristic diagram showing the dependence of silicon oxide film thickness on the gas

pressure of the processing chamber;
FIG.8 is a characteristic diagram showing the depth distribution profile of the Kr density ion the silicon oxide film;
FIG.9 is a characteristic diagram showing the current versus voltage characteristic of the silicon oxide film;
FIG.10 is a diagram showing the relationship between the leakage current of the silicon oxide film and the silicon oxynitride film and the film thickness;
FIGS.11A - 11C are diagrams showing the formation method of a nitride film and a fabrication method of a semiconductor device according to a second embodiment of the present invention;
FIG.12 is a characteristic diagram showing the dependence of the silicon nitride film thickness on the gas pressure of the processing chamber;
FIGS.13A - 13D are diagrams showing the formation method of an oxide/nitride laminated dielectric film and a fabrication method of a semiconductor device according to a third embodiment of the present invention;
FIG.14 is a diagram showing the nitrogen distribution in the oxide/nitride laminated dielectric film;
FIG.15 is a band structure diagram of the oxide/nitride laminated dielectric film;
FIGS.16A - 16C are diagrams showing the formation method of an oxynitride film and a fabrication method of a semiconductor device according to a fourth embodiment of the present invention;
FIG.17 is a diagram showing the photoemission intensity of atomic state oxygen and atomic state hydrogen at the time of formation of the oxynitride film;
FIG.18 is a diagram showing the elemental distribution profile in the silicon oxynitride film;
FIG.19 is a characteristic diagram showing the current versus voltage characteristic of the silicon oxynitride film;
FIG.20 is a schematic diagram showing the time-dependent change of nitrogen in the silicon nitride film;
FIGS.21A - 21C are schematic diagrams showing the shallow trench isolation according to a fifth embodiment of the present invention;
FIG.22 is a cross-sectional diagram of a three-dimensional transistor formed on a silicon surface having projections and depressions according to the fifth embodiment of the present invention;
FIG.23 is a diagram showing the construction of a flash memory device according to a sixth embodiment of the present invention;
FIG. 24 is a band structure diagram showing the writing operation of the flash memory device of FIG. 23;
FIG.25 is a diagram showing the leakage current characteristics of the tunneling insulation film in the flash memory device of FIG.23;
FIG.26 is a schematic diagram showing the cross-sectional structure of a flash memory device according to a seventh embodiment of the present invention;
FIGS.27-30 are schematic cross-sectional diagrams showing the fabrication process of the flash memory device of FIG.26 step by step;
FIG. 31 is a schematic diagram showing the cross-sectional structure of a MOS transistor formed on a metal substrate SOI according to an eighth embodiment of the present invention;
FIG.32 is a schematic diagram of a plasma processing apparatus according to a ninth embodiment of the present invention applicable to a glass substrate or plastic substrate;
FIG.33 is a schematic diagram showing the cross-sectional structure of a polysilicon transistor on an insulation film formed according to the plasma processing apparatus of FIG.32; and
FIG.34 is a schematic diagram showing the cross-sectional diagram of a three-dimensional LSI according to a tenth embodiment of the present invention.

BEST MODE FOR IMPLEMENTING THE INVENTION

[0044] Hereinafter, various preferable embodiments to which the present invention is applied will be explained in detail with reference to the drawings.

(FIRST EMBODIMENT)]

[0045] FIGS.4A - 4C show the low-temperature formation process of an oxide film that uses plasma as well as the fabrication process of a semiconductor device that uses such an oxide film according to a first embodiment of the present invention. Further, FIG.5 shows an example of a plasma processing apparatus used in the present invention and having a radial line slot antenna in a cross-sectional view.

[0046] In the present embodiment, the hydrogen terminating the dangling bonds at a silicon surface is first removed in the step of FIG. 4A. More specifically, the removal process of the surface-terminating hydrogen and the oxidation process are conducted in the same processing chamber continuously, and the Kr gas, which is used for the plasma excitation gas in the subsequent oxide film formation process, is used in the removal process of the surface-terminating hydrogen.

[0047] First, a vacuum vessel (processing chamber) 101 is evacuated in the plasma processing apparatus of FIG.5 and an Ar gas is introduced first from a shower plate 102. Then, the gas is changed to the Kr gas. Further, the pressure inside the processing chamber 101 is set to about 133Pa (1Torr).

[0048] Next, a silicon substrate 103 is placed on a stage 104 having a heating mechanism, and the temperature of the specimen is set to about 400°C. As long as the temperature of the silicon substrate 103 is in the

range of 200-500°C, the same results explained as below are obtained. It should be noted that the silicon substrate 103 is subjected to a treatment in a diluted hydrofluoric acid in the preprocessing step immediately before, and as a result, the dangling bonds on the surface of the silicon substrate are terminated by hydrogen.

[0049] Next, a microwave of 2.45GHz is supplied to a radial line slot antenna 106 from a coaxial waveguide 105 with the frequency of 2.45GHz, wherein the microwave thus supplied is introduced into the processing chamber 101 from the radial line slot antenna 106 through a dielectric plate 107 provided on a part of the wall of the processing chamber 101. The microwave thus introduced cause excitation of the Kr gas introduced into the processing chamber 101 from the shower plate 102, and as a result, there is induced high-density Kr plasma right underneath the shower plate 102. As long as the frequency of the microwave thus supplied is in the range of about 900MHz or more but not exceeding about 100GHz, almost the same results explained as below are obtained.

[0050] In the construction of FIG.5, the separation between the shower plate 102 and the substrate 103 is set to 6cm in the present embodiment. Smaller the gap separation, the film formation rate becomes faster. Further, while the present embodiment shows the example of film formation by using the plasma apparatus that uses a radial line slot antenna, it should be noted that the plasma may be induced by introducing the microwave into the processing chamber by other ways.

[0051] By exposing the silicon substrate 103 to the plasma thus excited by the Kr gas, the surface oc the silicon substrate 103 experiences bombardment of low energy Kr ions, and as a result, the surface-terminating hydrogen are removed.

[0052] FIG.6 shows the result of analysis of the silicon-hydrogen bond on the surface of the silicon substrate 103 by means of infrared spectrometer and shows the effect of removal of the surface-terminating hydrogen at the silicon surface by the Kr plasma induced by introducing the microwave into the processing chamber 101 under the pressure of 133Pa (1Torr) with the power of 1.2W/cm^2.

[0053] Referring to FIG.6, it can be seen that the optical absorption at about 2100cm^{-1}, which is characteristic to the silicon-hydrogen bond, is more or less vanished after the Kr plasma radiation conducted for only 1 second. Further, after continuous irradiation for thirty seconds, this optical absorption is almost completely vanished. This means the surface-terminating hydrogen on the silicon surface can be removed by the Kr plasma irradiation conducted for about 30 seconds. In the present embodiment, the surface-terminating hydrogen is completely removed by conducting the Kr plasma irradiation for 1 minute.

[0054] Next, in the step of FIG.4B, a Kr/O_2 mixed gas is introduced from the shower plate 102 with a partial pressure ratio of 97/3. Thereby, the pressure of the processing chamber is maintained at about 133Pa (1 Torr). In the high-density excitation plasma in which the Kr gas and the O_2 gas are mixed, Kr* in the intermediate excitation state and the O_2 molecules cause collision and there is caused efficient formation of atomic state oxygen O* in large amount.

[0055] In the present embodiment, the atomic state oxygen O* thus formed are used for oxidizing the surface of the silicon substrate 103, and as a result, there is formed an oxide film 103A. In the thermal oxidation process conducted conventionally on a silicon surface, the oxidation is caused by the 02 molecules or H_2O molecules and a very high temperature of 800°C or more has been needed. In the oxidation processing of the present invention conducted by the atomic state oxygen O*, the oxidation becomes possible at a very low temperature of about 400°C. In order to facilitate the collision of Kr* and O_2, it is preferable to use a high pressure for the pressure of the processing chamber. However, the use of excessively high pressure facilitates mutual collision of O* thus formed, and the atomic state oxygen O* thus formed are returned to the O_2 molecules. Thus, there exists an optimum gas pressure.

[0056] FIG.7 shows the relationship between the thicknesses of the oxide film 103A thus formed and the internal pressure of the processing chamber for the case the pressure inside the processing chamber 101 is changed while maintaining the Kr/O_2 pressure ratio to 97/3. In FIG.7, the temperature of the silicon substrate 103 is set to 400°C and the oxidation processing is conducted for 10 minutes.

[0057] Referring to FIG. 7, it can be seen that the oxidation rate becomes maximum in the case the pressure inside the processing chamber 101 is about 133Pa (1 Torr) and that this pressure or the pressure condition near this is the optimum condition. This optimum pressure is not limited to the case in which the silicon substrate 103 has the (100) surface orientation but is valid also in other cases in which the silicon surface has any other surface orientations.

[0058] After the silicon oxide film 103A is thus formed to the desired film thickness, the introduction of the microwave power is shutdown and the plasma excitation is terminated. Further, the Kr/O_2 mixed gas is replaced with the Ar gas, and with this, the oxidation processing is terminated. It should be noted that the use of the Ar gas before and after the foregoing step is intended to enable the use of low-cost Ar gas cheaper than Kr for the purging gas. The Kr gas used in the present step is recovered and reused.

[0059] Following the foregoing oxide film formation process, the gate electrode 103B is formed on the oxide film 103A, and a semiconductor integrated circuit device including transistors and capacitors is formed after conducting various patterning processing, ion implantation processing, passivation film formation processing, hydrogen sintering processing, and the like.

[0060] The result of measurement of hydrogen con-

tent in the silicon oxide film formed according to the foregoing process indicates that the hydrogen content is about $10^{22}/cm^2$ or less in terms of surface density in the case the silicon oxide film has a thickness of 3nm, wherein it should be noted that the foregoing measurement was conducted by measuring the hydrogen release caused with temperature rise. Particularly, it was confirmed that the oxide film characterized by a small leakage current shows that the hydrogen content in the silicon oxide film is about $10^{11}/cm^2$ or less in terms of surface density. On the other hand, the oxide film not exposed to the Kr plasma before the oxide film formation contained hydrogen with the surface density exceeding $10^{12}/cm^2$.

[0061] Further, the comparison was made on the roughness of the silicon surface before and after the oxide film formation conducted according to the process noted before wherein the measurement of the surface roughness was made by using an atomic force microscope. It should be noted that the silicon surface was exposed after the oxide film formation, by removing the silicon oxide film thus formed. It was confirmed that there is caused no change of surface roughness. Thus, there is caused no roughening of silicon surface even when the oxidation processing is conducted after the removal of the surface-terminating hydrogen.

[0062] FIG.8 shows the depth profile of Kr density in the silicon oxide film formed according to the foregoing process as measured by the total reflection X-ray fluorescent spectrometer. It should be noted that FIG.7 shows the result for the silicon (100) surface, while this result is not limited to the (100) surface and a similar result is obtained also in other surface orientations.

[0063] In the experiment of FIG.8, the partial pressure of oxygen in Kr is set to 3% and the pressure of the processing chamber is set to 133Pa (133 Torr). Further, the plasma oxidation processing is conducted at the substrate temperature of 400°C.

[0064] Referring to FIG.8, the Kr density in the silicon oxide film increases with increasing distance from the silicon surface and reaches the value of about $2 \times 10^{11}/cm^2$ at the surface of the silicon oxide film. This indicates that the silicon oxide film obtained according to the foregoing processing is a film in which the Kr concentration is constant in the film in the region in which the distance to the underlying silicon surface is 4nm or more and in which the Kr concentration decreases toward the silicon/silicon oxide interface in the region within the distance of 4nm from the silicon surface.

[0065] FIG.9 shows the dependence of the leakage current on the applied electric field for the silicon oxide film obtained according to the foregoing process. It should be noted that the result of FIG.9 is for the case in which the thickness of the silicon oxide film is 4.4nm. For the purpose of comparison, FIG.9 also shows the leakage current characteristic in which no exposure to the Kr plasma was conducted before the formation of the oxide film.

[0066] Referring to FIG.9, the leakage current characteristic of the silicon oxide film not exposed to the Kr plasma is equivalent to the leakage current characteristic of the conventional thermal oxide film. This means that the Kr/O_2 microwave plasma processing does not improve the leakage current characteristics of the oxide film thus obtained very much. On the other hand, in the case the oxidation processing is conducted by the present embodiment in which the Kr/O_2 gas is introduced after the Kr plasma irradiation processing, it can be seen that the leakage current is improved by the order of 2 or 3 as compared with the leakage current of the silicon oxide film formed by the conventional microwave plasma oxidation processing when measured at the same electric field, indicating that the silicon oxide film formed by the present embodiment has excellent low leakage characteristics. It is further confirmed that a similar improvement of leakage current characteristic is achieved also in the silicon oxide film having a much thinner film thickness of 1.7nm.

[0067] FIG.10 shows the result of measurement of the leakage current characteristics of the silicon oxide film of the present embodiment for the case the thickness of the silicon oxide film is changed variously. In FIG.10, Δ shows the leakage current characteristic of a conventional thermal oxide film, O shows the leakage current characteristic of the silicon oxide film formed by conducting the oxidation processing by the Kr/O2 plasma while omitting the exposure process to the Kr plasma, while ● shows the leakage current characteristic of the silicon oxide film of the present embodiment in which the oxidation is conducted by the Kr/O_2 plasma after exposure to the Kr plasma. In FIG. 9, it should be noted that the data represented by ■ shows the leakage current characteristic of an oxynitride film to be explained later.

[0068] Referring to FIG.10, it can be seen that the leakage current characteristic of the silicon oxide film represented by O and formed by the plasma oxidation processing while omitting the exposure process to the Kr plasma coincides with the leakage current characteristic of the thermal oxide film represented by Δ, while it can be seen also that the leakage current characteristics of the silicon oxide film of the present embodiment and represented by ● is reduced with respect to the leakage current characteristics represented by O by the order of 2-3. Further, it can be seen that a leakage current of $1 \times 10^{-2}A/cm^2$, which is comparable to the leakage current of the thermal oxide film having the thickness of 2nm, is achieved in the silicon oxide film of the present embodiment in the case the oxide film has the thickness of about 1.5nm.

[0069] Further, the measurement of the surface orientation dependence conducted on the silicon/silicon oxide interface state density for the silicon oxide film obtained by the embodiment of the present invention has revealed the fact that a very low interface state density of about $1 \times 10^{10}cm^{-2}eV^{-1}$ is obtained for any silicon sur-

face of any surface orientation.

[0070] Further, the oxide film formed by the present embodiment shows equivalent or superior characteristics as compared with the conventional thermal oxide film with regard to various electric and reliability characteristics such as breakdown characteristics, hot carrier resistance, charge-to-breakdown electric charges QBD, which corresponds to the electric charges up to the failure of the silicon oxide film under a stress current, and the like.

[0071] As noted above, it is possible to form a silicon oxide film on a silicon surface of any surface orientation at a low temperature of 400°C by conducting the silicon oxidation processing by the Kr/O2 high-density plasma after removal of the terminating hydrogen. It thought that such an effect is achieved because of the reduced hydrogen content in the oxide film caused as a result of the removal of the terminating hydrogen and because of the fact that the oxide film contains Kr. Because of the reduced amount of hydrogen in the oxide film, it is believed that weak element bonding is reduced in the silicon oxide film. Further, because of the incorporation of Kr in the film, the stress inside the film and particularly at the Si/SiO_2 interface is relaxed, and there is caused a reduction of trapped electric charges or reduction of interface state density. As a result, the silicon oxide film shows significantly improved electric properties.

[0072] Particularly, it is believed that the feature of reducing the hydrogen concentration in the film to the level of $10^{12}/cm^2$ or less, preferably to the level of $10^{11}cm^2$ or less, and the feature of incorporation of Kr into the film with a concentration of $5 \times 10^{11}/cm^2$ or less are thought as contributing to the improvement of electric properties and reliability of the silicon oxide film.

[0073] In order to realize the oxide film of the present invention, it is also possible to use a plasma processing apparatus other than the one shown in FIG.5, as long as the plasma processing apparatus can conduct the oxide film formation at low temperatures by using plasma. For example, it is possible to use a two-stage shower plate-type plasma processing apparatus in which there are provided a first gas release structure for releasing Kr for plasma excitation by a microwave and a second gas release structure different from the first gas release structure for releasing the oxygen gas.

[0074] In the present embodiment, it should be noted that the feeding of the microwave power is shutdown upon formation of the silicon oxide film to a desired film thickness, followed by the process of replacing the Kr/O_2 mixed gas with the Ar gas. On the other hand, it is also possible to introduce a Kr/NH_3 mixed gas from the shower plate 102 with the partial pressure ratio of 98/2 before shutting down the microwave power while maintaining the pressure at about 133Pa (1 Torr). Thereby, a silicon nitride film of about 0.7nm thickness is formed on the surface of the silicon oxide film upon termination of the processing. According to such a process, it becomes possible to form an insulation film having a higher specific dielectric constant by forming a silicon oxynitride film in which a silicon nitride film is formed on the surface thereof.

(SECOND EMBODIMENT)

[0075] FIGS. 11A - 11C show the formation method of a nitride film at low temperature by using plasma according to a second embodiment of the present invention, as well as the fabrication method of a semiconductor device that uses such a nitride film.

[0076] In the present embodiment, too, an apparatus similar to the one shown in FIG.5 is used for the nitride film formation. Further, in the present embodiment, it is preferable to use Ar or Kr for the plasma excitation gas for removing the terminating hydrogen and for the nitride film formation, in order to form a high-quality nitride film.

[0077] Hereinafter, an example of using Ar will be represented.

[0078] First, the interior of the vacuum vessel (processing chamber) 101 of FIG.5 is evacuated to a vacuum state in the step of FIG. 11A and an Ar gas is introduced from the shower plate 102 such that the pressure inside the processing chamber is set to about 13.3Pa (100mTorr).

[0079] Next, a silicon substrate 103 is introduced into the processing chamber 101 and is placed on the state 104 in which there is provided a heating mechanism, wherein the silicon substrate is subjected to a cleaning process conducted in a hydrogenated water and the silicon dangling bonds at the substrate surface are terminated by hydrogen. Further, the temperature of the specimen is set to 500°C. As long as the temperature is in the range of 300-550°C, results similar to the one described below are obtained.

[0080] Next, a microwave of 2.45GHz is supplied into the processing chamber from the coaxial waveguide 105 via the radial line slot antenna 106 and the dielectric plate 107 and a high-density plasma of Ar is induced in the processing chamber. As long as the frequency of the supplied microwave is in the range of about 900MHz or more but not exceeding about 10GHz, results similar to the one described below are obtained. In the present embodiment, the separation between the shower plate 102 and the substrate 103 is set to 6 cm. With decreasing separation, faster deposition rate becomes possible. While the present embodiment shows the example of film formation by a plasma apparatus that uses the radial line slot antenna, it is also possible to introduce the microwave into the processing chamber by other methods.

[0081] The silicon surface thus exposed to the plasma excited based on an Ar gas is subjected to bombardment of low energy Ar ions, and the surface-terminating hydrogen are removed as a result. In the present embodiment, the Ar plasma exposure process is conducted for 1 minute.

[0082] Next, in the step of FIG.11B, an NH_3 gas is mixed to the Ar gas from the shower plate 102 with a

partial pressure ratio of 2%. Thereby, the pressure of the processing chamber is held at about 13.3Pa (100mTorr). In high-density plasma in which the Ar gas and the NH_3 gas are mixed, there are caused collision of Ar* in the intermediate excited state and the NH_3 molecules, and NH* radicals are formed efficiently. The NH* radicals thus formed cause nitridation of the silicon substrate surface, and as a result, there is formed a silicon nitride film 103 on the surface of the silicon substrate 103.

[0083] Upon formation of the silicon nitride film 103C with a predetermined thickness, the supply of the microwave power is shutdown and the excitation of the plasma is terminated. Finally, the Ar/NH_3 mixed gas is replaced with the Ar gas and the nitridation processing is terminated.

[0084] Further, in the step of FIG. 11C, the silicon nitride film 103C thus formed by the nitride film formation process in the step of FIG. 11C is used as a gate insulation film and the gate electrode 103D is formed on the gate insulation film 103C. Further, various patterning processes, ion implantation processes, passivation film formation processes, hydrogen sintering processes, and the like are conducted, and a semiconductor integrated circuit that includes therein transistors and capacitors is obtained.

[0085] While the present embodiment showed the case in which the nitride film is formed by the plasma processing apparatus that uses the radial line slot antenna, it is also possible to introduce the microwave into the processing chamber by other ways. Further, while the present embodiment uses Ar for the plasma excitation gas, similar results are obtained also when Kr is used. Further, while the present embodiment uses NH_3 for the process gas, it is also possible to use a mixed gas of N_2 and H_2 for this purpose.

[0086] In the silicon nitride film formation process of the present invention, it is important that there remains hydrogen in the plasma even after the surface-terminating hydrogen are removed. As a result of existence of hydrogen in the plasma, the dangling bonds inside the silicon nitride film as well as the dangling bond on the interface are terminated by forming Si-H bonds or N-H bond, and a result, electron traps are eliminated from the silicon nitride film and the interface.

[0087] The existence of the Si-H bond and the N-H bond is confirmed respectively by infrared absorption spectroscopy and by X-ray photoelectron spectroscopy. As a result of existence of hydrogen, the hysteresis in the CV characteristics is eliminated and the interface state density at the silicon/silicon nitride film is suppressed to $2 \times 10^{10} cm^{-2}$. In the case of forming the silicon nitride film by using a rare gas (Ar or Kr) and an N_2/H_2 mixed gas, it is possible to suppress the traps of electrons or holes in the film drastically by setting the partial pressure of the hydrogen gas to 0.5% or more.

[0088] FIG.12 shows the pressure dependence of the silicon nitride film thickness formed according to the process noted above. In the experiment of FIG.12, it should be noted that the Ar/NH_3 partial pressure ratio was set to 98/2 and the deposition was conducted for 30 minutes.

[0089] Referring to FIG. 12, it can be seen that there occurs an increase of deposition rate of the nitride film by reducing the pressure in the processing chamber and thus by increasing the energy given to NH_3 (or N_2/H_2) . Thus, from the viewpoint of efficiency of nitride film formation, it is preferable to set the gas pressure to the range of 6.65 - 13.3Pa (50 - 100mTorr). On the other hand, from the viewpoint of productivity, it is preferable to use a unified pressure suitable to the oxidation processing such as 133Pa (1 Torr), particularly in the case of conducting the oxidation processing and the nitridation processing continuously, as will be explained with reference to other embodiments. Further, it is preferable to set the partial pressure of NH_3 (or N_2/H_2) in the rare gas to the range of 1-10%, more preferably to the range of 2 - 6%.

[0090] It should be noted that the silicon nitride film 103C thus obtained by the present embodiment showed the specific dielectric constant of 7.9, while this value is about twice as large as the specific dielectric constant of a silicon oxide film.

[0091] Measurement of the current versus voltage characteristics of the silicon nitride film 103C obtained by the present embodiment has revealed the fact that the film shows a leakage current characteristic smaller by the order of 5 - 6 than that of a thermal oxide film having the thickness of 1.5nm in the case the film has a thickness of 3.0nm (equivalent to the oxide film thickness of 1.5nm), under the condition that a voltage of 1V is applied. This means that it is possible to break through the limitation of miniaturization that appears in the conventional transistors that use a silicon oxide film for the gate insulation film, by using the silicon nitride film of the present embodiment.

[0092] Further, it should be noted that the film formation condition of the nitride film noted above as well as the physical and electrical properties are not limited to the case of forming the silicon nitride film on the (100) oriented silicon surface but are valid also in the case of forming the silicon nitride film on the silicon of any surface orientation including the (111) surface.

[0093] It should be noted that the preferable results achieved by the present embodiment are not only attained by the removal of the terminating hydrogen but also by the existence of Ar or Kr in the nitride film. Thus, in the nitride film of the present embodiment, it is believed that Ar or Kr relaxes the stress inside the nitride film or at the silicon/nitride film interface. As a result, the fixed electric charges in the nitride film or the interface state density is reduced, and this contributed also to the remarkable improvement of the electric properties and the reliability of the nitride film.

[0094] Particularly, it is thought that the existence of Ar or Kr with the surface density of 5 x 1011/cm2 or less

is effective for the improvement of the electric properties and reliability of the silicon nitride film, just like the case of the silicon oxide film.

[0095] In order to realize the nitride film 103C of the present invention, it is also possible to use other plasma processing apparatus than the one shown in FIG. 5, as long as it enables low temperature oxide film formation by using plasma. For example, it is possible to use a two-stage shower plate type plasma processing apparatus that includes a first gas release structure for releasing an Ar or Kr gas for excitation of plasma by microwave and a second gas release structure different from the first gas release structure for releasing the NH_3 (or N_2/H_2) gas.

(THIRD EMBODIMENT)

[0096] FIGS.13A - 13D show the formation method of a two-layer laminated dielectric structure according to a third embodiment of the present invention in which an oxide film and nitride film formed by the low-temperature plasma process are laminated, as well as a fabrication process of a semiconductor device that uses such a two-layer laminated dielectric structure.

[0097] It should be noted that the apparatus used for the formation of the oxide film and the nitride film in the present embodiment is identical with the apparatus of FIG. 5. In the present embodiment, Kr is used for the plasma excitation gas at the time of formation of the oxide film and the nitride film.

[0098] First, in the step of FIG.13A, the vacuum vessel (processing chamber) 101 is evacuated to the vacuum state and an Ar gas is introduced into the processing chamber 101 from the shower plate 102. Next, the gas to be introduced the next is switched to the Kr gas from the initial Ar gas, and the pressure of the processing chamber 101 is set to about 133Pa (1 Torr).

[0099] Next, the silicon substrate 103, preprocessed in the preprocessing step immediately before by conducting the diluted hydrofluoric acid treatment for terminating the surface dangling bonds of silicon by hydrogen, is introduced into the processing chamber 101 and placed on the stage 104 having a heating mechanism. Further, the temperature of the specimen is set to 400°C.

[0100] Next, a microwave of 2.45GHz frequency is introduced to the radial line slot antenna 106 from the coaxial waveguide 105 for 1 minute, wherein the microwave thus supplied is introduced into the processing chamber 101 via the dielectric plate 107. Thereby, there is induced high-density Kr plasma in the processing chamber 101, and the surface-terminating hydrogen is removed by exposing the surface of the silicon substrate 103 to the plasma.

[0101] Next, in the step of FIG.13B, the pressure inside the processing chamber 101 is maintained at 133Pa (1 Torr) and a Kr/O2 mixed gas is introduced from the shower plate 102 with the partial pressure ratio of 97/3. Thereby, there is formed a silicon oxide film 103A on the surface of the silicon substrate 103 with a thickness of 1.5nm.

[0102] Next, in the step of FIG.13C, the supply of the microwave is shutdown momentarily and supply of the O_2 gas is terminated. After purging the interior of the vacuum vessel (processing chamber) 101 with Kr, a mixed gas of Kr/NH_3 is introduced from the shower plate 103 with a partial pressure ratio of 98/2. Further, the pressure of the processing chamber is set to about 133Pa (1 Torr) and the microwave of 2.56GHz is introduced again to form the high-density plasma in the processing chamber 101. With this, a silicon nitride film 103N is formed on the surface of the silicon oxide film 103A with the thickness of 1nm.

[0103] Upon formation of the silicon nitride film 103A with the desired thickness, the microwave power is shutdown and the plasma excitation is terminated. Further, the Kr/NH_3 mixed gas is replaced with the Ar gas and the oxynitridation processing is terminated.

[0104] Next, in the step of FIG.13D, the oxynitride film thus obtained is used for the gate insulation film and a gate electrode 103B is formed thereon. Further, by conducting various patterning processing, ion injection processing, passivation film formation processing, hydrogen sintering processing, and the like, a semiconductor integrated circuit having transistors or capacitors is obtained.

[0105] Measurement of the effective dielectric constant conducted on such a laminated gate insulation film ahs revealed the value of about 6. Further, the film showed excellent electric properties and reliability such as leakage current characteristic, breakdown characteristic, hot-carrier resistance, similarly to the case of the first embodiment. The gate insulation film thus obtained showed no dependence of surface orientation of the silicon substrate 103, and excellent gate insulation film was formed also on the silicon of any surface orientation other than the (100) surface.

[0106] While the present embodiment explained the two-layer construction in which an oxide film located closer to the silicon side and a nitride film are laminated, it is also possible to change the order of lamination of the oxide film and the nitride film depending on the propose. Further, it is also possible to form the structure of plural laminated films such as oxide/nitride oxide, nitride/oxide/nitride, and the like.

[0107] FIG.14 shows the nitrogen concentration distribution in the two-layer laminated structure obtained by the present embodiment.

[0108] Referring to FIG. 14, it can be seen that there is caused concentration of nitrogen in correspondence to the nitride film 103N at the depth of 2-3nm from the surface of the dielectric film, while there occurs no further penetration of nitrogen. Thus, according to the present embodiment, it is possible to form a nitride region at the oxide film surface with the thickness of 2-3nm stably.

[0109] FIG.15 shows the band structure of the semiconductor device of FIG.13D taken along the cross-section A-A' for the thermal equilibrium state.

[0110] Referring to FIG.15, there is formed a nitride layer 103N of small bandgap adjacent to the silicon oxide layer 103A of large bandgap, and the gate electrode 103B is formed adjacent to the nitride film layer 103N. Further, the silicon substrate 103 exists adjacent to the silicon oxide film layer 103A.

[0111] In such a band structure, it should be noted that the conduction electrons in the silicon substrate 103 are blocked by the thick dielectric film formed of the silicon oxide film 103A and the nitride film 103N as long as the semiconductor device is in the non-driving state in which no voltage is applied to the gate electrode 103A, and there is caused no leakage of the conduction electrons tot eh gate electrode 103A. As will be explained later with reference to the flash memory device, the band structure of FIG.15 is extremely effective for suppressing the leakage current and simultaneously increasing the current density of the tunneling current.

(FOURTH EMBODIMENT)

[0112] FIG.16A - 16C show the formation method of an oxynitride film conducted at low temperature by using plasma according to a fourth embodiment of the present invention and a fabrication process of a semiconductor device that uses such an oxynitride film. It should be noted that the oxynitride film formation apparatus used in the present embodiment is identical with the one shown in FIG.5. In the present embodiment, Kr is used for the plasma excitation gas.

[0113] First, the interior of the vacuum vessel (processing camber 101) of FIG.5 is evacuated to the vacuum state in the step of FIG. 16A, and an Ar gas is introduced into the processing chamber 101 from the shower plate 102. Next, the gas introduced to the processing chamber 101 is switched to a Kr gas from the Ar gas, and the pressure inside the processing chamber is set to about 133Pa(1 Torr).

[0114] Further, the silicon substrate 103, preprocessed in the preprocessing step conducted immediately before by a diluted hydrofluoric treatment for terminating the dangling bonds of silicon on the surface by hydrogen, is introduced into the processing chamber 101 and is placed on the stage 104 having a heating mechanism. Further, the temperature of the specimen is set to 400°C.

[0115] Next, a microwave of 2.45GHz frequency is supplied to the radial line slot antenna 106 from the coaxial waveguide 105 for 1 minute, wherein the microwave thus supplied is introduced into the processing chamber 107 from the radial lien slot antenna 106 through the dielectric plate 107. Thereby, there is formed high-density plasma of Kr in the processing chamber 101. The surface-terminating hydrogen is thus removed by exposing the surface of the silicon substrate 103 to the plasma thus excited on the Kr gas.

[0116] Next, in the step of FIG.16B, the pressure of the processing chamber 101 is maintained at about 133Pa (1 Torr) and a mixed gas of $Kr/O_2/NH_3$ is introduced from the shower plate 103 with the partial pressure ratio of 96.5/3/0.5. Thereby, a silicon oxynitride film 103E is formed on the silicon surface with the thickness of 3.5nm. Upon formation of the silicon oxynitride film of the desire film thickness, the supply of the microwave power is shutdown and the plasma excitation is terminated. Further, the $Kr/O_2/NH_3$ mixed gas is replaced with the Ar gas and the oxynitridation processing is terminated.

[0117] Next, in the step of FIG.16C, the oxynitride film 103E thus formed is used for the gate insulation film, and a gate electrode 103F is formed on the gate insulation film 103E. Further, by conducting various patterning processes, ion implantation processes, passivation film formation processes, hydrogen sintering processes, and the like, are conducted, and a semiconductor integrated circuit device having transistors and capacitors is obtained.

[0118] FIG. 17 shows the relationship between the density of atomic state oxygen O* formed in the processing apparatus of FIG.5 measured by photoemission analysis and the mixing ratio of the NH_3 gas in the $Kr/O_2/NH_3$ gas.

[0119] Referring to FIG.17, the density of the atomic state oxygen O* as measured by the photoemission analysis does not change substantially when the mixing ratio of the $Kr/O_2/NH_3$ gas is in the range of 97/3/0 - 95/3/2, while when the ratio of NH_3 is increased further, the formation of the atomic state oxygen O* is reduced and the amount of the atomic state hydrogen is increased. Particularly, in the oxynitride film obtained in the case the mixing ratio of the $Kr/O2/NH_3$ gas is about 96.5/3/0.5, it can be seen that the leakage current becomes minimum and both of the breakdown voltage and the resistance against electric charge injection are improved.

[0120] FIG.18 shows the concentration distribution of silicon, oxygen and nitrogen in the oxynitride film of the present embodiment as measured by a secondary ion mass spectrometer, wherein the horizontal axis of FIG. 18 shows the depth as measured from the surface of the oxynitride film. In FIG.18, it can be seen that the distribution of silicon, oxygen and nitrogen is changing gently in the film, while this merely means non-uniformity of etching and does not mean that the thickness of the oxynitride film is non-uniform.

[0121] Referring to FIG.18, it can be seen that the concentration of nitrogen in the oxynitride film is large at the silicon/silicon oxynitride film interface and also at the silicon oxynitride film surface and decreases at the central part of the oxynitride film. Thereby, it should be noted that the amount of nitrogen incorporated into the oxynitride film is several ten percent as compared with silicon or oxygen. As will be explained later, the nitrogen

concentrating to the silicon/silicon oxynitride film interface in the silicon oxynitride film of FIG. 18 is thought as relaxing the stress at such an interface. As a result of such stress relaxation, the trapping of electric charges in the film or the density of interface states caused by the stress is reduced in the silicon oxynitride film of FIG. 18, and this contributes to the reduction of the leakage current.

[0122] FIG.19 shows the dependence of leakage current of the oxynitride film of the present embodiment on the applied electric field, wherein FIG.19 also shows the leakage current characteristic of the oxide film of the same film thickness in which the exposure process to the Kr plasma is omitted before the oxide film formation process by the microwave plasma and further the leakage current characteristic of the oxide film formed by a thermal oxidation process for the purpose of comparison.

[0123] Referring to FIG.19, it can be seen that the value of the leakage current at the same electric field is reduced by the order of 2 - 4 in the oxynitride film of the present embodiment in which the oxynitridation processing is conducted by introducing the $Kr/O_2/NH_3$ gas after removing the terminating hydrogen by the Kr plasma irradiation as compared with the oxide film formed by the conventional process and that the oxynitride film thus formed has excellent low-leakage characteristics.

[0124] In FIG.10 explained before, it should be noted that the relationship of the leakage current characteristic and the film thickness of the oxynitride film thus formed is represented by ■.

[0125] Referring to FIG. 10 again, the oxynitride film formed by the present embodiment after conducting the Kr irradiation has a similar leakage characteristic to the oxide film formed with a similar process and that the leakage current is only $1 \times 10^{-2} A/cm^2$ also in the case the film thickness is about 1.6nm.

[0126] It should be noted that the oxynitride film of the present embodiment also showed excellent electric properties and reliability such as breakdown characteristic and hot carrier resistance superior to the oxide film of the first embodiment explained before. Further, there was observed no dependence on the surface orientation of the silicon substrate, and thus, it becomes possible to form a gate insulation film of excellent characteristic not only on the (100) surface of silicon but also on the silicon surface of any surface orientation.

[0127] As explained above, it becomes possible to form a silicon oxynitride film of superior characteristics and film quality on the silicon surface of any surface orientation at the low temperature of 400°C by conducting the silicon oxynitridation processing by using the $Kr/O_2/NH_3$ high-density plasma, after removing the surface-terminating hydrogen.

[0128] The reason why such advantageous effect can be achieved by the present embodiment is attributed not only to the reduction of hydrogen content in the oxynitride film caused by removal of the surface-terminating hydrogen but also to the effect of the nitrogen contained in the oxynitride film with a proportion of several ten percent or less. In the oxynitride film of the present embodiment, the content of Kr is about 1/10 or less as compared with the oxide film of the first embodiment, and in place of Kr, the film contains a large amount of nitrogen. Thus, in the present embodiment, it is believed that the reduction of hydrogen in the oxynitride film causes reduction of weak bonds in the silicon oxynitride film, while the existence of nitrogen in the film caused relaxation of stress in the film or at the si/SiO_2 interface. As a result of this, the number of trapped electrical charges in the film or the surface state density is reduced, and the electric properties of the oxynitride film is improved significantly. Particularly, it is believed the reduction of hydrogen concentration level in the oxynitride film to $10^{22} cm^{-2}$ or less, more preferably $10^{11} cm^{-2}$ or less and the existence of nitrogen in the film with a proportion of several ten percent with respect to silicon or oxygen contribute to the improvement of the electric properties and reliability of the silicon oxynitride film.

[0129] In the present embodiment, the supply of the microwave power is shutdown at the end of the oxynitridation processing upon formation of the silicon oxynitride film with the predetermined thickness, and the $Kr/O_2/NH_3$ mixed gas is replaced with the Ar gas. On the other hand, it is possible to terminate the oxynitridation processing by introducing a Kr/NH3 mixed gas with the partial pressure ratio of 98/2 from the shower plate 103 before the shutdown of the microwave power while maintaining the pressure at 133Pa (1 Torr) and form a silicon nitride film on the surface of the silicon oxynitride film with the thickness of about 0.7nm. According to this process, a silicon nitride film is formed on the surface of the silicon oxynitride film and an insulation film having a higher dielectric constant is obtained.

[0130] In the oxynitride film of the present embodiment, it should be noted that the concentration of nitrogen to the silicon/oxynitride film interface and the concentration of nitrogen to the surface of the oxynitride film explained with reference to FIG.18 are maintained during the growth of the oxynitride film.

[0131] FIG.20 shows the change of the nitride distribution profile with the growth of the oxynitride film schematically.

[0132] Referring to FIG.20, nitrogen concentrate to the surface of the oxynitride film and to the interface between the oxynitride film and the underlying silicon substrate, and this tendency is maintained even when the oxynitride film has made a growth. As a result, the oxynitride film, while having an overall composition of an oxynitride film, does have a composition near an oxide film in the mid depth part of the film and a composition near a nitride film at the surface as well at the interface between the oxynitride film and the substrate. Further, the depth of penetration of nitrogen at the oxynitride film is limited to 2-3nm or less, and thus, the thickness of the

nitride film formed on the surface of the oxynitride film is limited to 2-3nm.

(FIFTH EMBODIMENT)

[0133] Next, formation process of a semiconductor device according to a fifth embodiment of the present invention will be described wherein the semiconductor device includes a high-quality silicon oxide film formed on a corner part of the device isolation sidewall that constitutes a shallow-trench isolation or on a silicon surface having an undulating surface form.

[0134] FIG.21A shows the concept of shallow trench isolation.

[0135] Referring to FIG.21A, the illustrated shallow trench isolation is formed by forming an isolation trench on a surface of a silicon substrate 1003 by conducting a plasma etching process, filling the trench thus formed with a silicon oxide film 1002 formed by a CVD process, and planarizing the silicon oxide film 1002 by a CMP process, and the like.

[0136] In the present embodiment, the silicon substrate is exposed to an oxidizing atmosphere at 800 - 900°C after the polishing step of the silicon oxide film 1002 to conduct sacrifice oxidation process, and the silicon oxide film thus formed as a result of the sacrifice oxidation process is etched away in a chemical solution containing hydrofluoric acid. Thereby, a silicon surface terminated with hydrogen is obtained. In the present embodiment, a procedure similar to the one explained in the first embodiment is conducted and the surface-terminating hydrogen is removed by using the Kr plasma. Thereafter, the Kr/O2 gas is introduced and the silicon oxide film is formed with the thickness of about 2.5nm.

[0137] According to the present embodiment, the silicon oxide film is formed with a uniform thickness even on the corner part of the shallow trench isolation without causing decrease of silicon oxide film thickness. The silicon oxide film thus formed by the plasma oxidation process while using the Kr plasma has excellent QBD (charge-to-breakdown) characteristics including the shallow trench isolation part, and there is caused no increase of leakage current even in the case the injected electric charges are 10^2C/cm^2. Thus, the reliability of the device is improved significantly.

[0138] In the case of forming the silicon oxide film by the conventional thermal oxidation process, the thickness of the silicon oxide film is severely reduced at the corner part of the shallow trench isolation with increasing taper angle of the shallow trench isolation, while in the case of the present invention, no such thinning of the silicon oxide film is caused at such a corner part of the shallow trench isolation even in the case the taper angle is increased. Thus, in the present embodiment, the use of a near rectangular taper angle for the trench of the shallow trench isolation structure enables reduction of the area of the device isolation region, and further increase of integration density becomes possible in the semiconductor device. It should be noted that the taper angle of about 70 degrees has been used for the device isolation part in the conventional technology, which relies on the thermal oxidation process, because of the limitation caused by the thinning of the thermal oxide film at the trench corner part as shown in FIG.21B. According to the present invention, it becomes possible to use the angle of 90 degrees.

[0139] FIG.22 shows the cross-sectional view of the silicon oxide film formed on a silicon surface in which an undulating surface morphology is formed by conducting a 90-degree etching, with a thickness of 3nm according to the procedure of the first embodiment.

[0140] Referring to FIG.22, it can be seen that a silicon oxide film of uniform thickness is formed on any of the surfaces.

[0141] The oxide film formed as such has excellent electric properties such as excellent leakage current or breakdown characteristic, and thus, the present invention can realize a high-density semiconductor integrated circuit having a silicon three-dimensional structure, which may include plural surface orientations as in the case of a vertical structure.

(SIXTH EMBODIMENT)

[0142] FIG.23 shows the construction of a flash memory device 20 according to a sixth embodiment of the present invention, wherein those parts corresponding to the parts described before are designated by the same reference numerals and the description thereof will be omitted.

[0143] Referring to FIG.23, the flash memory device 20 of the present embodiment uses the dielectric film 12A of the third embodiment or the fourth embodiment, for the tunneling insulation film 12.

[0144] FIG.24 shows the state in which a write voltage is applied to he control gate electrode 15 in the flash memory device 20 of FIG. 23.

[0145] Referring to FIG.24, it can be seen that the band structure of the silicon oxide film and the nitride film constituting the dielectric film 12A changes significantly upon application of the write voltage to the control gate electrode 15 due to the corresponding change of potential of the floating gate electrode 13, and the hot electrons formed in the channel region 11A are injected into the floating gate electrode 13 after passing through the triangular potential formed by the conduction band Ec of the silicon oxide film in the form of Fowler-Nordheim current.

[0146] As explained already with reference to FIG.15, such a dielectric film forms a thick potential barrier with regard to the conducting electrons in the channel region 11A in the non-writing state of the flash memory device 20, and the tunneling current is effectively blocked.

[0147] FIG.25 shows the voltage versus current characteristic of the tunneling insulation film 12A of the flash memory device 20 of FIG.25 in superposition with the

graph of FIG.3.

[0148] Referring to FIG.25, it can be seen that the tunneling insulation film 12A provides a very low leakage current in the case the applied electric field is small while the tunneling current increases sharply when the applied electric field is increased in response to application of a predetermined write voltage, and it becomes possible to conduct efficient writing of information in short time. Further, in the case of conducting the writing with the level of conventional injection current, the time needed for writing is reduced.

[0149] In the flash memory device 20 of FIG.23, the stress at the interface between the Si substrate 11 and the tunneling insulation film 12A is relaxed by using the oxynitride film 103E formed in the process of FIGS.16A - 16C for the tunneling insulation film 12A and the quality of the tunneling insulation film 12A is improved. As a result, the leakage current is reduced further. This means that the thickness of the tunneling insulation film 12A can be reduced, and thus, it becomes possible to realize a flash memory operating at low voltage.

(SEVENTH EMBODIMENT)

[0150] Next, a flash memory device according to a seventh embodiment of the present invention that uses the low-temperature formation technology of oxide film and nitride film or the low-temperature formation technology of oxynitride film by plasma will be explained. In the description below, it should be noted that the explanation is made on a flash memory device, while it should be noted that the present invention is applicable also to EPROMs and EEPROMs.

[0151] FIG.26 shows the schematic cross-sectional diagram of a flash memory device according to the present embodiment.

[0152] Referring to FIG.26, the flash memory device is constructed on a silicon substrate 1201 and includes a tunneling oxide film 1202 formed on the silicon substrate 1201, a first polysilicon gate electrode 1203 formed on the tunneling oxide film 1202 as a floating gate electrode, a silicon oxide film 1204 and a silicon nitride film 1205 formed consecutively on the polysilicon gate electrode 1203, and a second polysilicon gate electrode 1206 formed on the silicon nitride film 1205 as'a control gate electrode. In FIG.26, illustration of the source region, drain region, contact hole, interconnection patterns, and the like, is omitted. It should be noted that the silicon oxide film 1202 is formed by the silicon oxide film formation method explained with reference to the first embodiment, while the laminated structure of the silicon oxide film 1204 and the nitride film 1205 is formed by the formation method of silicon nitride film explained in relation to the third embodiment.

[0153] FIGS.27 - 30 are schematic diagrams explaining the fabrication process of the flash memory device of the present embodiment step by step.

[0154] Referring to FIG.27, a silicon substrate 1301 includes a flash memory cell region A, a high-voltage transistor region B and a low-voltage transistor region C such that the regions A - C are defined by a field oxide film 1302, wherein a silicon oxide film 1303 is formed on the surface of the silicon substrate 1301 in each of the regions A - C. The field oxide film 1302 may be formed by a selective oxidation process (LOCOS method) or shallow trench isolation method.

[0155] In the present embodiment, Kr is used for the plasma excitation gas for the removal of the surface-terminating hydrogen or for the formation of the oxide film and the nitride film. The same apparatus explained with reference to FIG.5 is used for the formation of the oxide film and the nitride film.

[0156] Next, in the step of FIG.28, the silicon oxide film 1303 is removed from the memory cell region A and the silicon surface is terminated by hydrogen by conducting the cleaning process in a hydrochloric acid solution. Further, a tunneling oxide film 1304 is formed similarly the first embodiment before.

[0157] Thus, the vacuum vessel (processing chamber) 101 is evacuated to the vacuum state similarly to the first embodiment and the Ar gas is introduced into the processing chamber 101 from the shower plate 102. Next, the Ar gas is switched to the Kr gas and the pressure inside the processing chamber 101 is set to about 1 Torr.

[0158] Next, the silicon oxide film 1303 is removed and the hydrofluoric acid treatment is applied to the silicon substrate. The silicon substrate 1301 thus processed is introduced into the processing chamber 101 as the silicon substrate 103 of FIG.5 and is placed on the stage 104 equipped with the heating mechanism. Further, the temperature of the substrate is set to 400°C.

[0159] Further, a microwave of 2.45GHz frequency is supplied from the coaxial waveguide 105 to the radial line slot antenna 106 for 1 minute, wherein the microwave thus supplied is introduced into the processing chamber 101 from the radial line slot antenna 106 through the dielectric plate 107. By exposing the surface of the silicon substrate to the high-density Kr plasma thus formed in the processing chamber 101, the terminating hydrogen are removed from the silicon surface of the substrate 1301.

[0160] Next, the Kr gas and the O_2 gas are introduced from the shower plate 102, and a silicon oxide film 1304 used for the tunneling insulation film is formed on the region A with a thickness of 3.5nm. Next, a first polysilicon layer 1305 is deposited so as to cover the silicon oxide film 1304.

[0161] Next, the first polysilicon layer 1305 is removed from the regions B and C for the high voltage and low voltage transistors by a patterning process, such that the first polysilicon pattern 1305 is left only on the tunneling oxide film 1304 in the memory cell region A.

[0162] After this etching process, a cleaning process is conducted and the surface of the polysilicon pattern 1305 is terminated with hydrogen.

[0163] Next, in the step of FIG.29, an insulation film 1306 having an ON structure and including a lower oxide film 1306A and an upper nitride film 1306B therein is formed so as to cover the surface of the polysilicon pattern 1305 similarly to the third embodiment.

[0164] More specifically, this ON film is formed as follows.

[0165] The vacuum vessel (processing chamber) 101 is evacuated to a vacuum state and the AR gas supplied from the shower plate 102 is switched to the Kr gas. Further, the pressure inside the processing chamber is set to about 133Pa (1 Torr). Next, the silicon substrate 1301 carrying thereon the polysilicon pattern 1305 in the state that the hydrogen termination is made is introduced into the processing chamber 101 and is placed on the stage 104 having the heating mechanism. Further, the temperature of the specimen is set to 400°C.

[0166] Next, a microwave of 2.45GHz frequency is supplied to the radial line slot antenna 106 from the coaxial waveguide 105 for about 1 minute. Thereby, the microwave is introduced into the processing chamber 101 from the radial line slot antenna 106 through the dielectric plate 107, and there is formed a high-density Kr plasma. As a result, the surface of the polysilicon pattern 1305 is exposed to the Kr gas and the surface terminating hydrogen is removed.

[0167] Next, a Kr/O2 mixed gas is introduced into the processing chamber 101 from the shower plate 102 while maintaining the pressure of the processing chamber 101 to 133Pa (1 Torr), and a silicon oxide film is formed on the polysilicon surface with a thickness of 3nm.

[0168] Next, the supply of the microwave is shutdown temporarily and introduction of the Kr gas and the O_2 gas is interrupted. Next, the interior of the vacuum vessel (processing chamber) 101 is evacuated and the Kr gas and an NH_3 gas are introduced from the shower plate 102. The pressure inside the processing chamber 101 is set to about 13.3Pa (100 mTorr) and the microwave of 2.45GHz is supplied again into the processing chamber 101 via the radial line slot antenna. Thereby, high-density plasma is formed in the processing chamber and a silicon nitride film is formed on the silicon oxide film surface with the thickness of 6nm.

[0169] Thus, there is formed an ON film with a thickness of 9nm, wherein it should be noted that the ON film thus obtained was extremely uniform characterized by a uniform film thickness, and no dependence on the polysilicon surface orientation was observed.

[0170] After such a process of formation of the ON film, the insulation film 1306 is removed from the regions B and C for the high-voltage and low-voltage transistors by conducting a patterning process in the step of FIG. 30, and ion implantation is conducted into the foregoing regions B and C of the high-voltage and low-voltage transistors for threshold control. Further, the oxide film 1303 is removed from the regions B and C and a gate oxide film 1307 is formed on the region B with a thickness of 5nm. Thereafter, a gate oxide film 1308 is formed on the region C with a thickness of 3nm.

[0171] After this, a second polysilicon layer 1309 and a silicide layer 1310 are formed consecutively on the entire structure including the field oxide film 1302, and there are formed gate electrodes 1311B and 1311C respectively in the high-voltage transistor region B and the low-voltage transistor region C by patterning the second polysilicon layer 1309 and the silicide layer 1310. Further, there is formed a gate electrode 1311A in correspondence to the memory cell region A.

[0172] After the step of FIG.30, source and drain regions are formed according to a standard semiconductor process, and the device is completed by further conducting formation of interlayer insulation films and contact holes and formation of wiring patterns.

[0173] In the present invention, it should be noted that the insulation films 1306A or 1306B maintains excellent electric properties even when the thickness thereof is reduced to about one half the conventional thickness of the oxide film or nitride film. Thus, these silicon oxide film 1306A and silicon nitride film 1306B maintains excellent electric properties even when the thickness thereof is reduced. Further, these films are dense and have high quality. Further, it should be noted that, because the silicon oxide film 1306A and the silicon nitride film 1306B are formed at low temperature, there arises no problem of thermal budget at the interface between the polysilicon gate and the oxide film, and excellent interface is realized.

[0174] The flash memory device of the present invention can perform the writing and erasing of information at low voltage, and because of this, the formation of substrate current is suppressed. Thereby, deterioration of the tunneling insulation film is suppressed. Thus, it becomes possible to produce a non-volatile semiconductor memory with high yield by arranging the flash memory of the present invention in a two-dimensional array. The non-volatile semiconductor memory apparatus thus formed shows stable characteristics.

[0175] Thus, the flash memory device of the present invention is characterized by small leakage current due to the excellent film quality of the insulation films 1306A and 1306B. Further, it becomes possible to reduce the film thickness without increasing the leakage current. Thus, it becomes possible to perform the writing operation or erasing operation at an operational voltage of about 5V. As a result, the memory retention time of the flash memory device is increase by the order of 2 or more as compared with the conventional device, and the number of possible rewriting operation is increase by the order of 2 or more.

[0176] It should be noted that the film structure of the insulation film 1306 is not limited to the ON structure explained above but it is also possible to use an O structure formed of an oxide film similar to that of the first embodiment or an N structure that uses a nitride film similar to the case of the second embodiment. Further,

it is possible to use an oxynitride film similar to the one shown in the fourth embodiment. Further, the insulation film 1306 may have an NO structure formed of a nitride film and an oxide film or an ONO structure in which an oxide film, a nitride film and an oxide film are laminated consecutively. Further, the insulation film 1306 may have an NONO structure in which a nitride film, an oxide film, a nitride film and an oxide film are laminated consecutively. Choice of any of the foregoing structures can be made according to the purpose from the viewpoint of compatibility with the gate insulation film used in the high voltage transistor or low voltage transistor in the peripheral circuit or from the viewpoint of possibility of shared use.

(EIGHTH EMBODIMENT)

[0177] It should be noted that the formation of the gate insulation film by using the foregoing Kr/O_2 microwave-excited high-density plasma or the formation of the gate nitride film by using the Ar (or Kr)/NH_3 (or N_2/H_2) microwave-excited high-density plasma, is advantageous to the formation of a semiconductor integrated circuit device on a silicon-on-insulator wafer including a metal layer in the underlying silicon (metal-substrate SOI). It should be noted that the use of high temperature process is not possible in such a metal-substrate SOI. Particularly, the effect of removal of the terminating hydrogen appears conspicuously in the SOI structure having a small silicon thickness and performing completely depleted operation.

[0178] FIG.31 shows the cross-section of a MOS transistor having a metal-substrate SOI structure.

[0179] Referring to FIG.31, 1701 is a low-resistance semiconductor layer of n+-type or p+-type, 1702 is a silicide layer such as NiSi, 1703 is a conductive nitride layer such as TaN or TiN, 1704 is a metal layer such as Cu, and the like, 1705 is a conductive nitride film such as TaN or TiN, 1706 is a low-resistance semiconductor layer of n+-type or p+-type, 1707 is a nitride insulation film such as AlN, Si_3N_4, and the like, 1708 is an SiO_2 film, 1709 is an SiO_2 layer or a BPSG layer or an insulation layer combining these, 1710 us a drain region of n+-type, 1711 us a source region of n+-type, 1712 is a drain region of p+-type, 1713 is a source region of p+-type, 1714 and 1715 are silicon semiconductor layers oriented in the <111> direction, 1716 is an SiO_2 film formed by the Kr/O_2 microwave-excited high-density plasma after removing the surface-terminating hydrogen by the procedure of the first embodiment of the present invention, 1717 and 1718 are respectively the gate electrodes of an n-MOS transistor and a p-MOS transistor and formed of Ta, Ti, TaN/Ta, TiN/Ti, and the like, 1719 is a source electrode of the n-MOS transistor, and 1720 is a drain electrode of the n-MOS transistor and a p-MOS transistor. Further, 1721 is a source electrode of a p-MOS transistor and 1722 is a substrate surface electrode.

[0180] In such a substrate including a Cu layer and protected by TaN or TiN, the temperature of thermal processing has to be about 700°C or less for suppressing diffusion of Cu. Thus, the source or drain region of n+-type or p+-type is formed by conducting a thermal annealing process at 550°C after ion implantation process of As+, AsF_2+ or BF_2+.

[0181] In the semiconductor device having the device structure of FIG.31, it should be noted that the comparison of the transistor sub-threshold characteristics between the case the gate insulation film is formed by a thermal oxide film and the case the gate insulation film is formed by the Kr/O_2 microwave-excited high-density plasma after removing the surface-terminating hydrogen by conducting the Kr plasma irradiation process, has revealed the fact that there appears kink or leakage in the sub-threshold characteristics when the gate insulation film is formed by the thermal oxidation process, while in the case the gate insulation film is formed by the present invention, excellent sub-threshold characteristics are obtained.

[0182] In the case a mesa-type device isolation structure is used, it should be noted that there appears a silicon surface having a surface orientation different from that of the silicon surface forming the flat part, at the sidewall part of the mesa device isolation structure. By forming the gate insulation film by the plasma oxidation process while using Kr, the oxidation of the mesa device isolation sidewall is achieved generally uniformly similarly to the flat part, and excellent electric properties and high reliability are achieved.

[0183] Further, it becomes possible to form a metal-substrate SOI integrated circuit device having excellent electric properties and high reliability also in the case of using a silicon nitride film formed by Ar/NH_3 according to the procedure of the second embodiment for the gate insulation film.

[0184] In the present embodiment, too, it is possible to obtain excellent electric characteristics even in the case the thickness of the silicon nitride film is set to 3nm (1.5nm in terms of silicon oxide film equivalent thickness), and the transistor drivability is improved by about twice as compared with the case of using a siliconoxide film of 3nm thickness.

(NINTH EMBODIMENT)

[0185] FIG.32 schematically shows an example of the fabrication apparatus according to an eighth embodiment of the present invention intended to conduct oxidation processing, nitridation processing or oxynitridation processing on a large rectangular substrate such as a glass substrate or a plastic substrate on which liquid crystal display devices or organic electro-luminescence devices are formed.

[0186] Referring to FIG.32, a vacuum vessel (processing chamber) 1807 is evacuated to a low pressure state and a Kr/O_2 mixed gas s introduced from a

shower plate 1801 provided in the processing chamber 1807. Further, the processing chamber 1807 is evacuated by a lead screw pump 1802 such that the pressure inside the processing chamber 1807 is set to 133Pa (1 Torr). Further, a glass substrate 1803 is placed on a stage 1804 equipped with a heating mechanism, and the temperature of the glass substrate is set to 300°C.

[0187] The processing chamber 1807 is provided with a large number of rectangular waveguides 1805 and a microwave is introduced into the processing chamber 1807 from respective slits of the foregoing rectangular waveguides 1805 via a dielectric plate 1806, and high-density plasma is formed in the processing chamber 1807. Thereby, the shower plate 1801 provided in the processing chamber 1807 functions also as a waveguide for propagating the microwave emitted by the waveguide in the right and left directions in the form of a surface wave.

[0188] FIG.33 shows an example of a polysilicon thin film transistor (TFT) used for driving a liquid crystal display device or an organic EL photoemission device or for use in a processing circuit, wherein it should be noted that the polysilicon thin film transistor of FIG.33 is formed by using the gate oxide film or gate nitride film of the present invention while using the apparatus of FIG.32.

[0189] First, the example of using a silicon oxide film will be explained.

[0190] Referring to FIG.33, 1901 is a glass substrate, 1902 is a Si_3N_4 film, 1903 is a channel layer of a polysilicon n-MOS transistor having a predominantly (111) orientation, 1905 and 1906 are respectively a source region and a drain region of the polysilicon n-MOS transistor, 1904 is a channel layer of a polysilicon p-MOS transistor having a predominantly (111) orientation, and 1907 and 1908 are respectively a source region and a drain region of the polysilicon p-channel MOS transistor. Further, 1901 is a gate electrode of the polysilicon n-MOS transistor while 1911 is a gate electrode of the polysilicon p-MOS transistor, 1912 is an insulation film such as SiO_2, BSG or BPSG, 1913 and 1914 are respectively the source electrode of the polysilicon n-MOS transistor (and simultaneously the drain electrode of the polysilicon p-MOS transistor), and 1915 is the source electrode of the polysilicon p-MOS transistor.

[0191] It should be noted that a polysilicon film formed on an insulation film takes a stable state when having the (111) surface orientation in the direction perpendicular to the insulation film. In this state, the polysilicon film is dense and well crystallized and thus provides high quality. In the present embodiment, it should be noted that 1909 is a silicon oxide film layer of the present invention formed by the procedure similar to the one explained with reference to the first embodiment by using the apparatus of FIG.32 and has a thickness of 0.2 μm. The oxide film 1909 is formed on the (111) oriented polysilicon at 400°C with a thickness of 3nm.

[0192] According to the present invention, there occurred no thinning of oxide film at the sharp corner part of the device isolation region formed between the transistors, and it was confirmed that the silicon oxide film is formed with uniform film thickness on the polysilicon film in any of the flat part and edge part. The ion implantation process for forming the source and drain regions was conducted without passing the ions through the gate oxide film, and the electrical activation was made at 400°C. As a result, the entire process can be conducted at a temperature of 400°C or less and formation of transistors became possible on a glass substrate. The transistor thus formed had the mobility of about 300cm^2/Vsec, or more for electrons and about 150cm^2/Vsec or more for holes. Further, a voltage of 12V or more was obtained for the source and drain breakdown voltages and for the gate breakdown voltage. Further, a high-speed operation exceeding 100MHz became possible in the transistor having the channel length of about 1.5-2.0nm. Further, it was confirmed that the silicon oxide film showed excellent leakage characteristics and excellent characteristics for the interface states formed at the polysilicon/oxide film interface.

[0193] By using the transistor of the present embodiment, the liquid crystal display devices or organic EL photoemission devices can provide various advantageous features such as large display area, low cost, high-speed operation, high reliability, and the like.

[0194] While the present embodiment is the one in which the gate insulation film or the gate nitride film of the present invention is applied to a polysilicon, the present embodiment is applicable also to the gate oxide film or gate insulation film of an amorphous silicon thin-film transistor (TFT) or staggered-type thin-film transistor (TFT), which is used in a liquid crystal display device and the like.

(TENTH EMBODIMENT)

[0195] Next, an embodiment of a three-dimensional stacked LSI in which an SOI device having a metal layer, a polysilicon device and an amorphous silicon device are stacked will be described.

[0196] FIG.34 show the cross-section of the three-dimensional LSI of the present invention schematically.

[0197] Referring to FIG.34, 2001 is a first SOI device and wiring layer, 2002 is a second SOI device and a wiring layer, 2003 is a first polysilicon device and a wiring layer, 2004 is a second polysilicon device and a wiring layer, while 2005 is a layer of an amorphous semiconductor device and a functional-material device and includes a wiring layer thereof.

[0198] In the first SOI and wiring layer 2001 and also in the second SOI and wiring layer 2002, there are formed various parts such as digital processing parts, high-precision and high-speed analog parts, synchronous DRAM parts, power supply parts, interface circuit parts, and the like, by using the SOI transistors explained with reference to the seventh embodiment.

[0199] In the first polysilicon device and wiring layer 2003, there are formed various parallel digital processing parts, inter-functional block repeater parts, memory device parts, and the like, by using the polysilicon transistors or flash memories explained with reference to the sixth or eighth embodiments together with the wiring layer of the first polysilicon device layer 2003.

[0200] In the second polysilicon device and wiring layer 2004, there are formed parallel analog processing parts such as an amplifier, A/D converter, and the like, by using the polysilicon transistor explained with reference to the eighth embodiment. Further, optical sensors, sound sensors, touch sensors, wireless transceiver parts, and the like, are formed in the amorphous semiconductor device/functional-material device and wiring layer 2005.

[0201] The signals formed by the optical sensors, sound sensors, touch sensors, wireless transceiver parts, and the like, provided in the amorphous semiconductor device/functional-material and wiring layer 2005 are processed by the parallel analog processing part such as an amplifier or A/D converter in the second polysilicon device and wiring layer 2004, and are forwarded further to the parallel digital processing parts and the memory device parts formed in the second polysilicon device and wiring layer 2004 by the polysilicon transistors and flash memory devices. The signals thus processed are then processed by the digital processing parts, high-precision and high-speed analog parts or the synchronous DRAM parts provided in the first SOI and wiring layer 2001 or second SOI and wiring layer 2002 by using the SOI transistors.

[0202] Further, the inter-functional block repeater part provided in the first polysilicon device and the wiring layer 2003 does not occupy a large area even when provided with plural numbers, and it is possible to achieve synchronization of signals all over the LSI.

[0203] It should be noted that such a three-dimensional LSI has become possible as a result of the technology explained in detail with reference to the embodiments.

INDUSTRIAL APPLICABILITY

[0204] According to the present invention, it becomes possible to form a tunneling oxide film on a silicon surface such as a silicon substrate in the form that an oxide film and a nitride film are laminated or a nitride film and an oxide film and a nitride film are laminated consecutively such that the tunneling oxide film as a whole as the composition of an oxynitride film. Thereby, the leakage current is reduced significantly while simultaneously reducing the film thickness. With this, it becomes possible to increase the tunneling current density of a flash memory device, and the like, at the time of writing, and the operational speed is improved. Further, the operational voltage is reduced.

Claims

1. A dielectric film formed on a silicon surface,
   said dielectric film containing nitrogen with a concentration distribution such that a nitrogen concentration increases at a dielectric film surface as compared to a central part of said dielectric film.

2. The dielectric film as claimed in claim 1, wherein said nitrogen concentration increases in said dielectric film also in the vicinity of an interface with said silicon surface as compared with a central part of said dielectric film.

3. The dielectric film as claimed in claim 1, wherein said dielectric film comprises a silicon oxynitride film, and wherein said nitrogen concentration becomes minimum at a central part of said film.

4. The dielectric film as claimed in claim 1, wherein said dielectric film substantially has a composition of a silicon nitride film at a film surface contacting with said electrode.

5. The dielectric film as claimed in claim 1, wherein said dielectric film substantially has a composition of a silicon oxide film at a central part of said film.

6. A semiconductor device, comprising:

   a silicon substrate;
   an insulation film formed on said silicon substrate; and
   an electrode formed on said insulation film,

   wherein said insulation film has a nitrogen concentration distribution such that a nitrogen concentration increases at a film surface contacting with said electrode as compared with a central part of said film.

7. The semiconductor device as claimed in claim 5, wherein said nitrogen concentration increases in said insulation film in the vicinity to an interface to said silicon substrate as compared with said central part.

8. The semiconductor device as claimed in claim 6, wherein said insulation film is a silicon oxynitride film, and wherein said nitrogen concentration becomes minimum at said central part of said film.

9. The semiconductor device as claimed in claim 6, wherein said insulation film substantially has a composition of a silicon nitride film at a film surface contacting with said electrode.

10. The semiconductor device as claimed in claim 6,

wherein said insulation film substantially has a composition of a silicon oxide film at said central part of said film.

11. The semiconductor device as claimed in claim 6, wherein there is further provided a second electrode on said first electrode via an inter-electrode insulation film.

12. A non-volatile semiconductor memory device, comprising:

a silicon substrate;
a tunneling insulation film formed on said silicon substrate;
a floating gate electrode formed on said tunneling insulation film; and
a control gate electrode formed on said floating gate electrode via an inter-electrode insulation film,
one of said insulation films having a nitrogen concentration distribution such that a nitrogen concentration increases at a film surface contacting with said electrode as compared with a central part of said film.

13. The non-volatile semiconductor device as claimed in claim 12, wherein said nitrogen concentration increases also in said tunneling insulation film near an interface to said silicon substrate as compared with said central part of said film.

14. The non-volatile semiconductor device as claimed in claim 12, wherein said tunneling insulation film is comprised of a silicon oxynitride film and wherein said nitrogen concentration becomes minimum at a central part of said film.

15. The non-volatile semiconductor device as claimed in claim 12, wherein said tunneling insulation film substantially has a composition of a silicon nitride film at a film surface contacting with said electrode.

16. The non-volatile semiconductor device as claimed in claim 1, wherein said tunneling insulation film substantially has a composition of a silicon oxide film at a central part of said film.

17. A method of forming a dielectric film, comprising the steps of:

forming a silicon oxide film on a surface;
modifying a surface of said silicon oxide film by exposing the same to hydrogen nitride radicals NH*.

18. The method of forming a dielectric film as claimed in claim 17, wherein said hydrogen nitride radicals NH* are formed by a microwave plasma formed in a mixed gas of an inert gas selected from Ar or Kr and a gas containing nitrogen and hydrogen as constituent elements.

19. The method of forming a dielectric film as claimed in claim 18, wherein said microwave plasma has an electron density of $10^{12}cm^{-2}$ or more at said surface.

20. The method of forming a dielectric film as claimed in claim 18, wherein said microwave plasma has a plasma potential of 10V or less at said surface.

21. The method of forming a dielectric film as claimed in claim 18, wherein said gas containing nitrogen and hydrogen as constituent elements comprises an NH_3 gas.

22. The method of forming a dielectric film as claimed in claim 18, wherein said gas containing said nitrogen and hydrogen is a mixed gas of a N_2 gas and a H_2 gas.

23. The method of forming a dielectric film as claimed in claim 17, wherein said surface comprises a silicon surface and said oxide film is formed by oxidation of said silicon surface.

24. The method of forming a dielectric film as claimed in claim 23, wherein said oxidation of said silicon surface is conducted by exposing said silicon surface to microwave plasma formed in a mixed gas of an inert gas predominantly of Kr and a gas containing oxygen as a constituent element.

25. The method of forming a dielectric film as claimed in claim 23, wherein said silicon oxide film is formed by thermal oxidation of said surface.

26. A method of forming a dielectric film, comprising the steps of:

forming a silicon oxide film on a surface; and
modifying a surface of said silicon oxide film by exposing the same to microwave plasma formed in a mixed gas of an inert gas selected from Ar or Kr and a gas containing nitrogen and hydrogen as constituent elements.

27. The method of forming a dielectric film as claimed in claim 26, wherein said microwave plasma has an electron density of $10^{12}cm^{-3}$ or more at said surface.

28. The method of forming a dielectric film as claimed in claim 26, wherein said microwave plasma has a plasma potential of 10V or less at said surface.

29. The method of forming a dielectric film as claimed in claim 26, wherein said gas containing said nitrogen and hydrogen as constituent elements comprises a NH_3 gas.

30. The method of forming a dielectric film as claimed in claim 26, wherein said gas containing nitrogen and hydrogen comprises a mixed gas of a N_2 gas and a H_2 gas.

31. The method of forming a dielectric film as claimed in claim 26, wherein said surface comprises a silicon surface and wherein said oxide film is formed by oxidation of said silicon surface.

32. The method of forming a dielectric film as claimed in claim 31, wherein said oxidation of said silicon surface is conducted by the step of exposing said silicon surface to microwave plasma formed in a mixed gas of an inert gas predominantly of Kr and a gas containing oxygen as a constituent element.

33. The method of forming a dielectric film as claimed in claim 31, wherein said silicon oxide film is formed by thermal oxidation of said silicon surface.

34. The method of forming a dielectric film comprising the step of exposing a silicon surface to microwave plasma formed in a mixed gas of an inert gas primarily formed of Kr, a gas containing nitrogen as a constituent element and a gas containing oxygen as a constituent element, to form an oxynitride film on said silicon surface.

35. The method of forming a dielectric film as claimed in claim 34, wherein said microwave plasma has an electron density of $10^{12}cm^{-3}$ or less at said silicon surface.

36. The method of forming a dielectric film as claimed in claim 34, wherein said microwave plasma has a plasma potential of 10V or less at said silicon surface.

37. The method of forming a dielectric film as claimed in claim 34, wherein said gas containing nitrogen as a constituent element comprises a NH_3 gas, and said gas containing oxygen as a constituent element comprises an O_2 gas.

38. The method of forming a dielectric film as claimed in claim 37, wherein said inert gas and said O_2 gas and said NH_3 gas are supplied with a partial pressure ratio of 96.5:3:0.5.

39. The method of forming a dielectric film as claimed in claim 34, wherein said silicon surface is exposed to said atomic state oxygen O* and hydrogen nitride radicals NH* in said step of exposing said silicon surface to said microwave plasma.

40. A method of fabricating a semiconductor device, comprising the steps of;

forming a silicon oxide film on a silicon substrate by an oxidation processing;

modifying a surface of said silicon oxide film by exposing the same to hydrogen nitride radicals NH^*; and

forming a gate electrode on said modified silicon oxide film.

41. The method of fabricating a semiconductor device as claimed in claim 34, wherein said hydrogen nitride radicals NH* are formed by microwave plasma formed in a mixed gas of an inert gas selected from Ar or Kr and a gas containing nitrogen and hydrogen as constituent elements.

42. The method of fabricating a semiconductor device as claimed in claim 41, wherein said microwave plasma has an electron density of $10^{12}cm^{-3}$ or more at said surface of said silicon substrate.

43. The method of fabricating a semiconductor device as claimed in claim 41, wherein said microwave plasma has a plasma potential of 10V or less at said surface of said silicon substrate.

44. The method of fabricating a semiconductor device as claimed in claim 41, wherein said gas containing nitrogen and hydrogen comprises a NH_3 gas.

45. The method of fabricating a semiconductor device as claimed in claim 41, wherein said gas containing nitrogen and hydrogen as constituent elements comprises a mixed gas of a N_2 gas and a H_2 gas.

46. The method of fabricating a semiconductor device as claimed in claim 41, wherein said silicon oxide film is formed by the step of exposing said silicon surface to microwave plasma formed in a mixed gas of an inert gas predominantly of Kr and a gas containing oxygen as a constituent element.

47. A method of fabricating a semiconductor device, comprising the steps of:

forming a silicon oxide film on a silicon substrate by an oxidation processing;

modifying a surface of said silicon oxide film by exposing the same to microwave plasma formed in a mixed gas of an inert gas selected from Ar or Kr and a gas containing nitrogen and hydrogen as constituent elements; and

forming a gate electrode on said modified silicon oxide film.

48. The method of fabricating a semiconductor device as claimed in claim 47, wherein said microwave plasma has an electron density of $10^{12}cm^{-3}$ or more at said surface of said silicon substrate.

49. The method of fabricating a semiconductor device as claimed in claim 47, wherein said microwave plasma has a plasma potential of 10V or less at said surface of said silicon substrate.

50. The method of fabricating a semiconductor device as claimed in claim 47, wherein said gas containing nitrogen and hydrogen as constituent elements comprises a NH_3 gas.

51. The method of fabricating a semiconductor device as claimed in claim 47, wherein said gas containing nitrogen and hydrogen as constituent elements comprises a mixed gas of a N_2 gas and a H_2 gas.

52. The method of fabricating a semiconductor device as claimed in claim 47, wherein oxidation of said silicon surface is conducted by the step of exposing said silicon surface to microwave plasma formed in a mixed gas of an inert gas of predominantly Kr and a gas containing oxygen as a constituent element.

53. The method of fabricating a semiconductor device as claimed n claim 47, wherein said silicon oxide film is formed by a thermal oxidation process.

54. A method of fabricating a semiconductor device, comprising the steps of:

exposing a silicon substrate surface to microwave plasma formed in a mixed gas of an inert gas primarily formed of Kr, a gas containing nitrogen as a constituent element and a gas containing oxygen as a constituent element, to form an oxynitride film on said silicon surface; and

forming a gate electrode on said oxynitride film.

55. The method of fabricating a semiconductor device as claimed in claim 54, wherein said microwave plasma has an electron density of $10^{12}cm^{-3}$ or more on said silicon substrate.

56. The method of fabricating a semiconductor device as claimed in claim 54, wherein said microwave plasma has a plasma potential of 10V or less on said silicon substrate.

57. The method of fabricating a semiconductor device as claimed in claim 54, wherein said gas containing nitrogen as a constituent element comprises a NH_3 gas, and said gas containing oxygen as a constituent element comprises an O_2 gas.

58. The method of fabricating a semiconductor device as claimed in claim 57, wherein said inert gas and said O_2 gas and said NH_3 gas are supplied to a partial pressure ratio of 96.5 : 3 : 0.5.

59. The method of fabricating a semiconductor device as claimed in claim 54, wherein said step of exposing said silicon surface of said microwave plasma comprises the step of exposing said silicon surface to atomic state oxygen O* and hydrogen nitride radicals NH*.

FIG.1

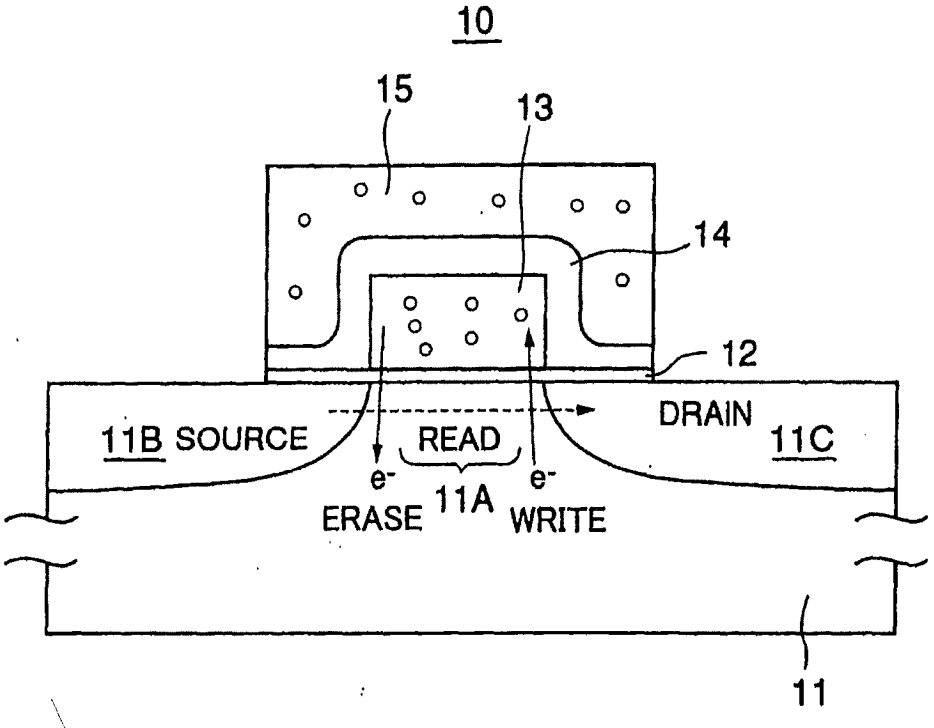


FIG.2A

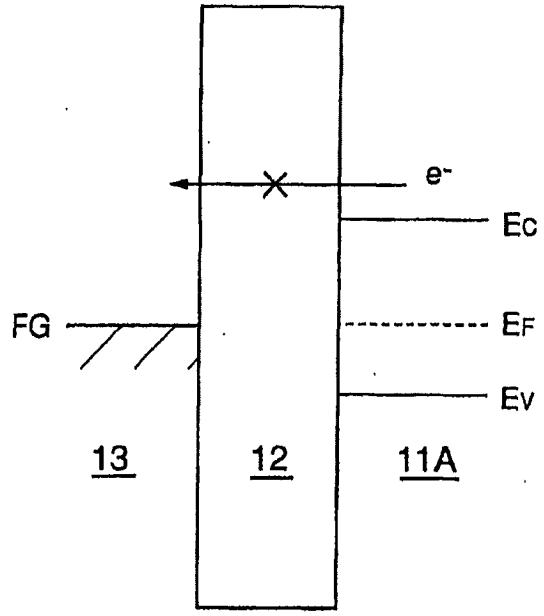


FIG.2B

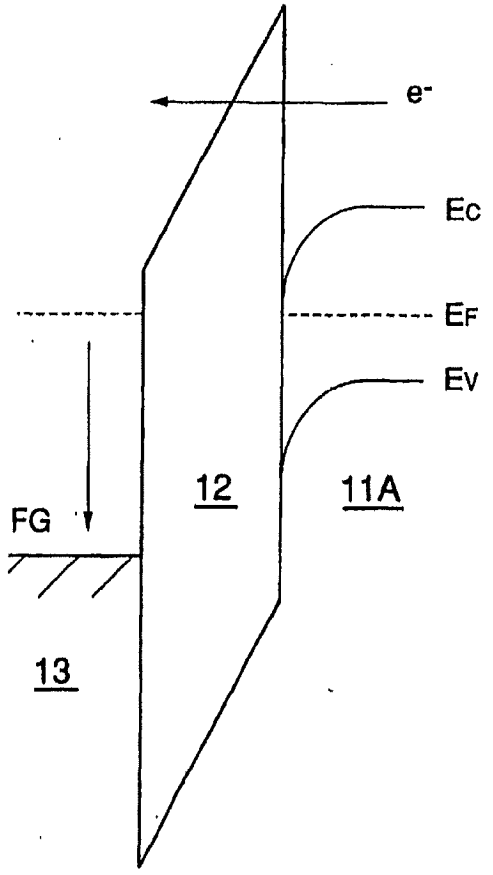


FIG.3

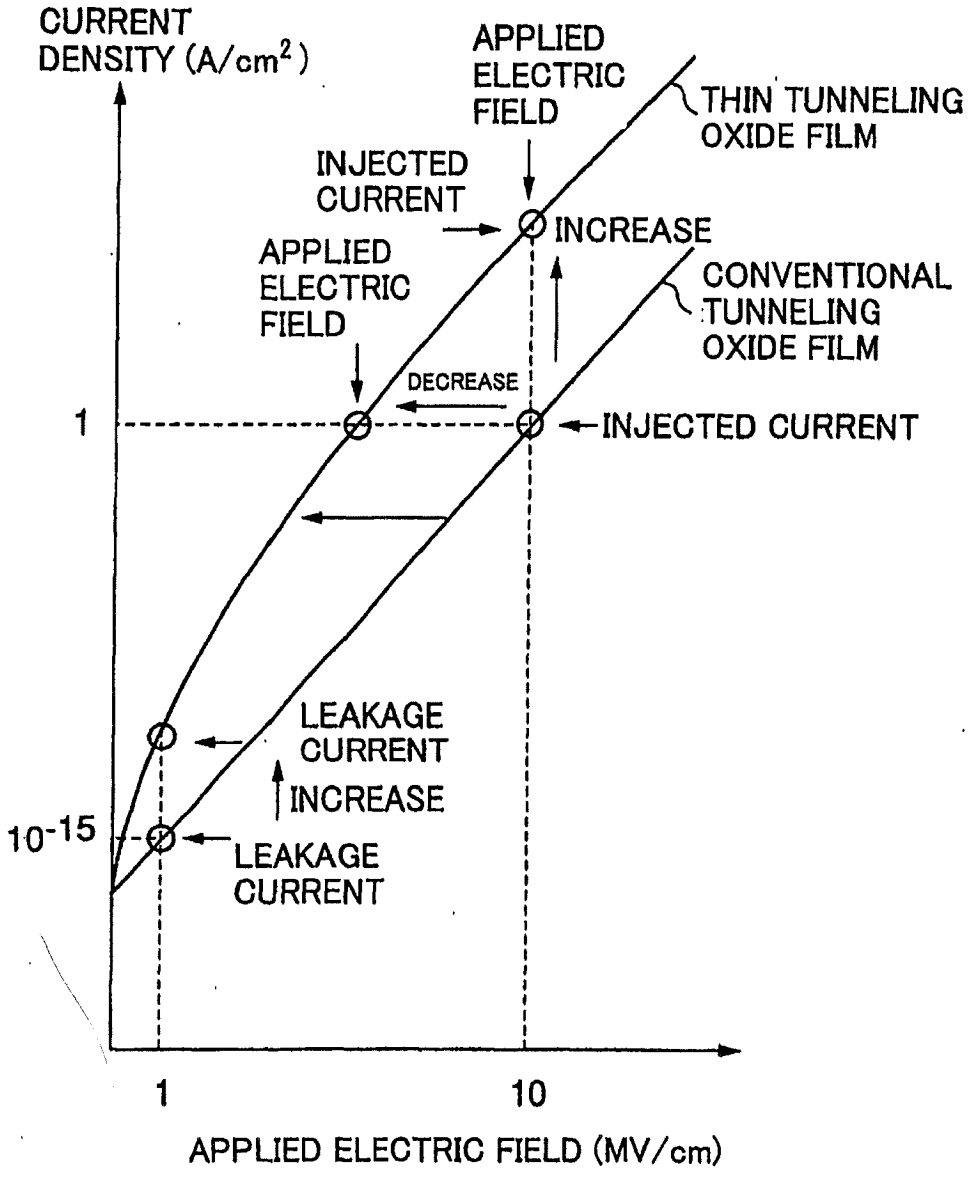

CURRENT DENSITY (A/cm²)
APPLIED ELECTRIC FIELD
THIN TUNNELING OXIDE FILM
INJECTED CURRENT
INCREASE
APPLIED ELECTRIC FIELD
CONVENTIONAL TUNNELING OXIDE FILM
DECREASE
1
INJECTED CURRENT
LEAKAGE CURRENT
INCREASE
10-15
LEAKAGE CURRENT
1
10
APPLIED ELECTRIC FIELD (MV/cm)

FIG.4A

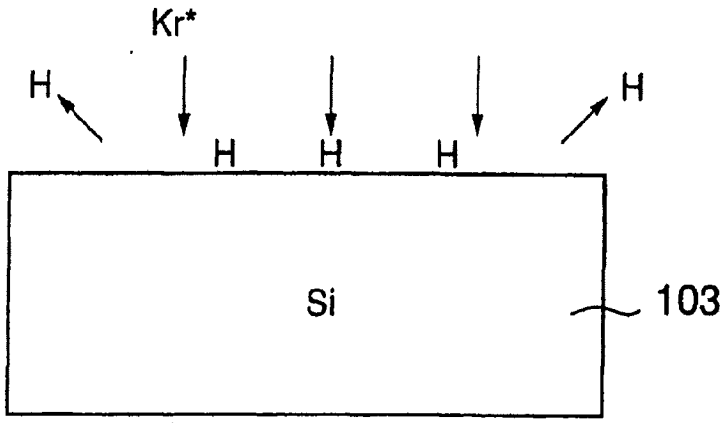


FIG.4B

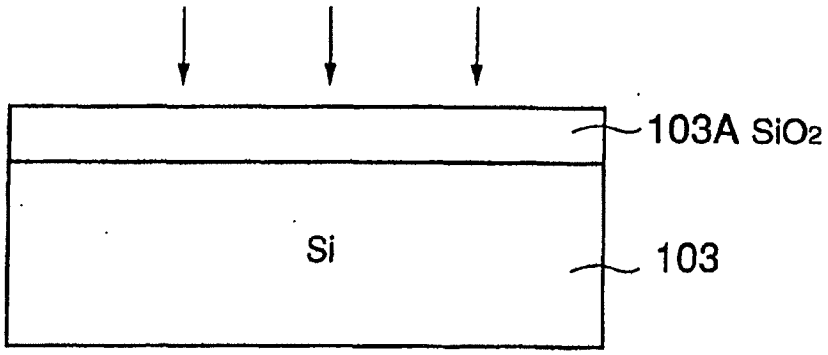


FIG.4C

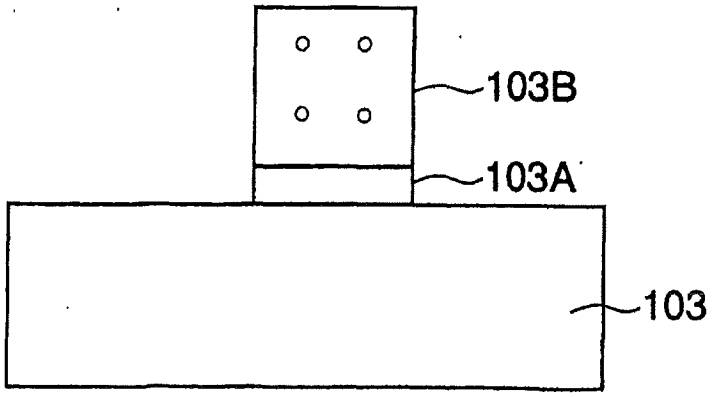


FIG.5

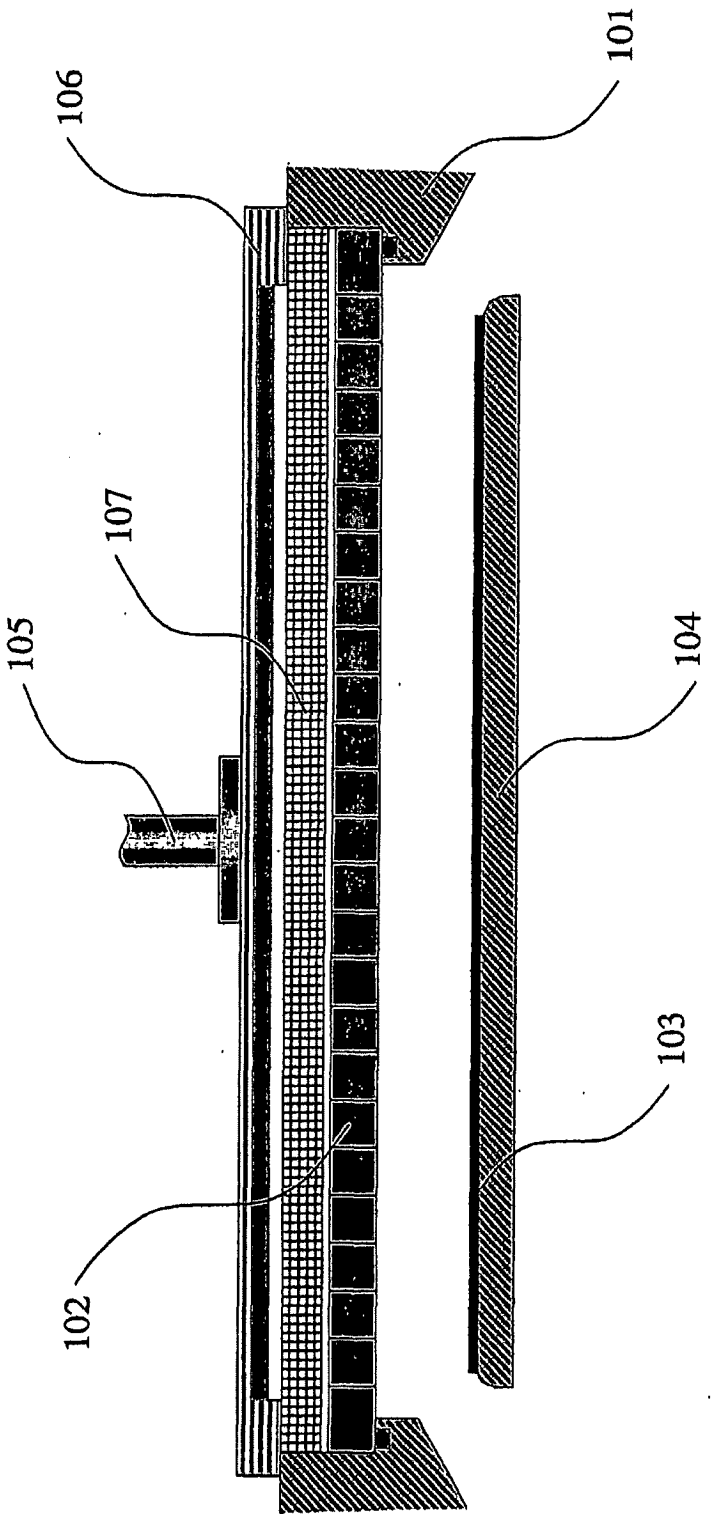


FIG.6

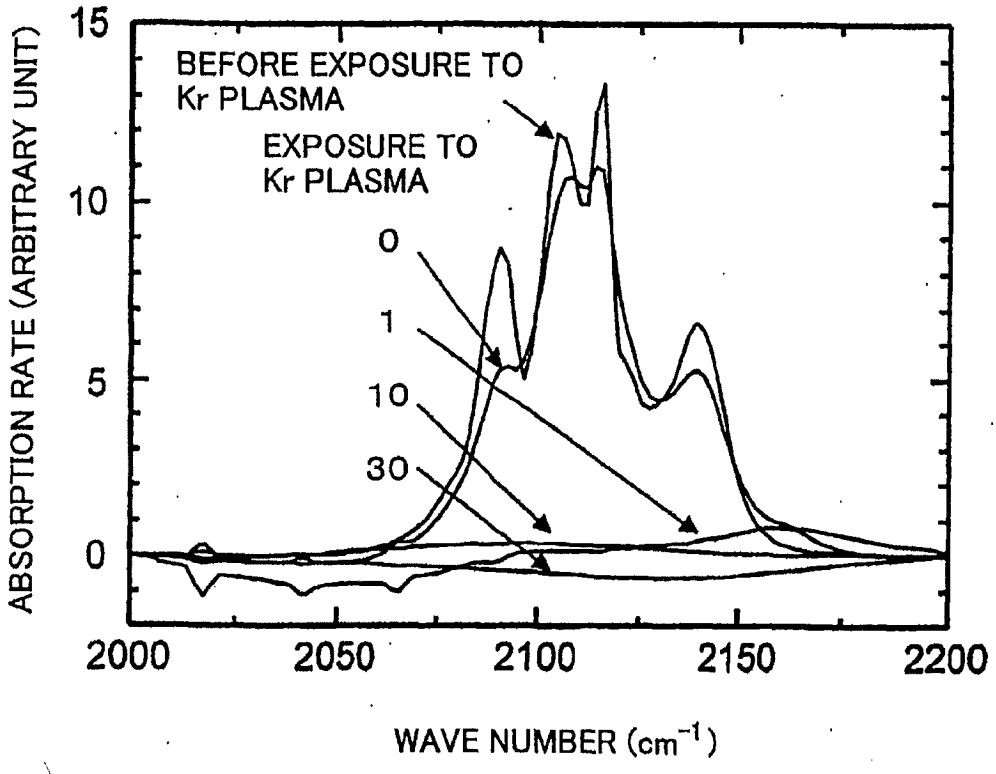

15
10
5
0
ABSORPTION RATE (ARBITRARY UNIT)
BEFORE EXPOSURE TO
Kr PLASMA
EXPOSURE TO
Kr PLASMA
0
1
10
30
2000
2050
2100
2150
2200
WAVE NUMBER (cm-1)

FIG.7

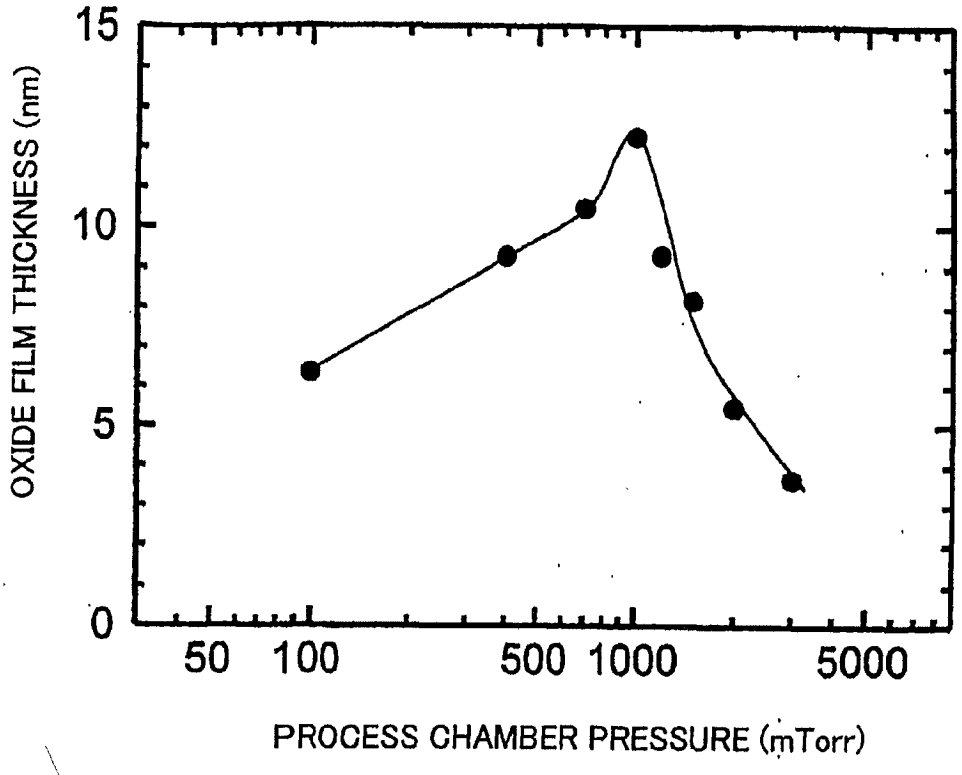

15
10
5
0
OXIDE FILM THICKNESS (nm)
50
100
500
1000
5000
PROCESS CHAMBER PRESSURE (mTorr)

FIG.8

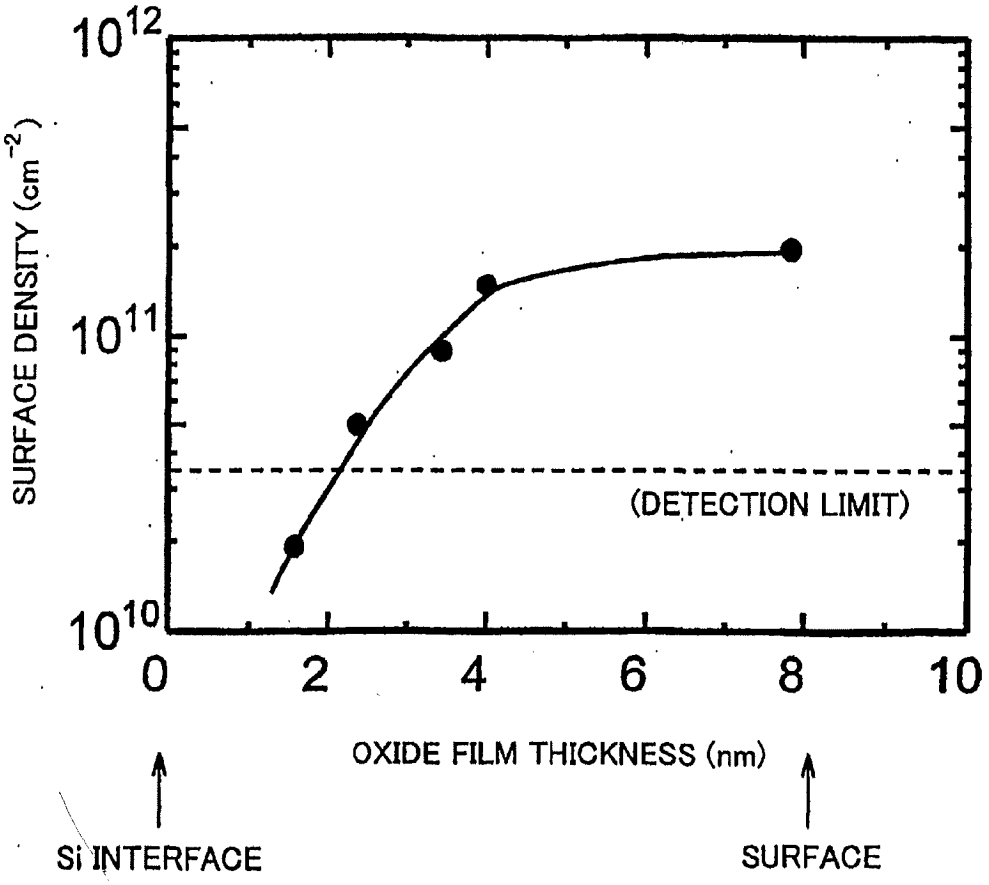

10^{12}
10^{11}
10^{10}
SURFACE DENSITY (cm^{-2})
(DETECTION LIMIT)
0
2
4
6
8
10
OXIDE FILM THICKNESS (nm)
Si INTERFACE
SURFACE

FIG.9

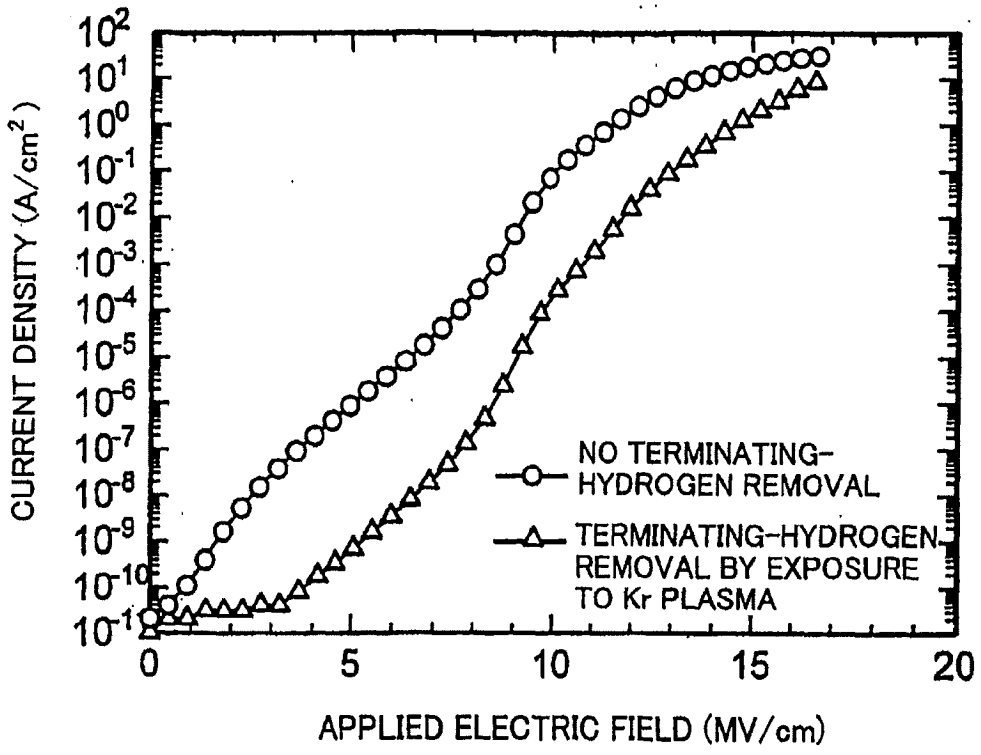

CURRENT DENSITY (A/cm²)
10²
10¹
10⁰
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
10⁻⁸
10⁻⁹
10⁻¹⁰
10⁻¹¹
0
5
10
15
20
APPLIED ELECTRIC FIELD (MV/cm)
NO TERMINATING-HYDROGEN REMOVAL
TERMINATING-HYDROGEN-REMOVAL BY EXPOSURE TO Kr PLASMA

FIG.10

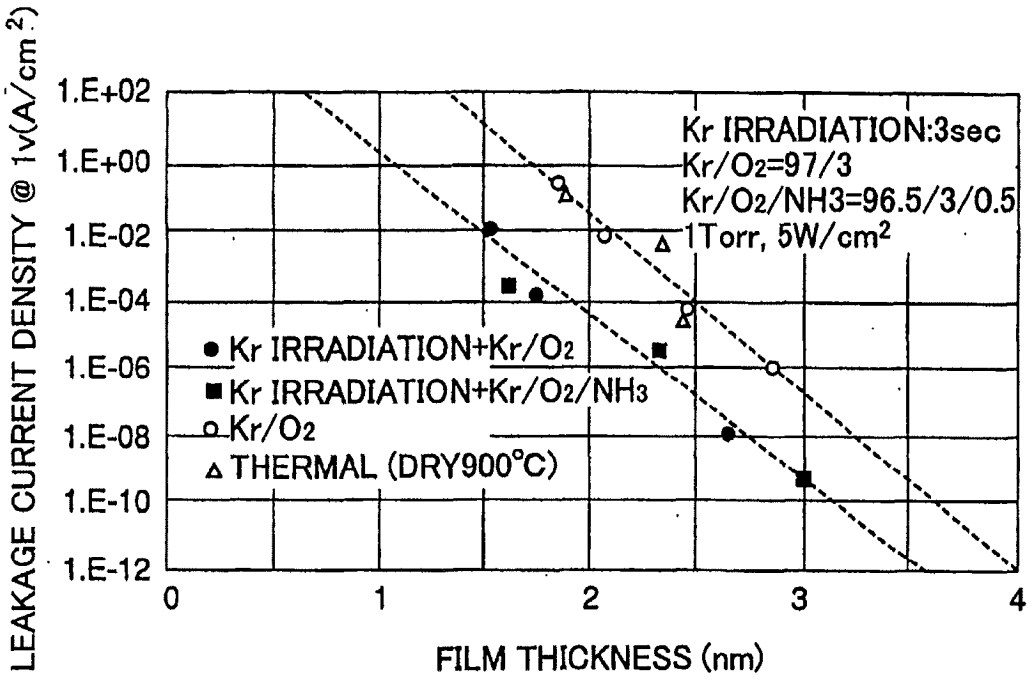

LEAKAGE CURRENT DENSITY @ 1v(A/cm²)
1.E+02
1.E+00
1.E-02
1.E-04
1.E-06
1.E-08
1.E-10
1.E-12
0
1
2
3
4
FILM THICKNESS (nm)
Kr IRRADIATION:3sec
Kr/O2=97/3
Kr/O2/NH3=96.5/3/0.5
1Torr, 5W/cm²
● Kr IRRADIATION+Kr/O2
■ Kr IRRADIATION+Kr/O2/NH3
○ Kr/O2
△ THERMAL (DRY900°C)

FIG.11A

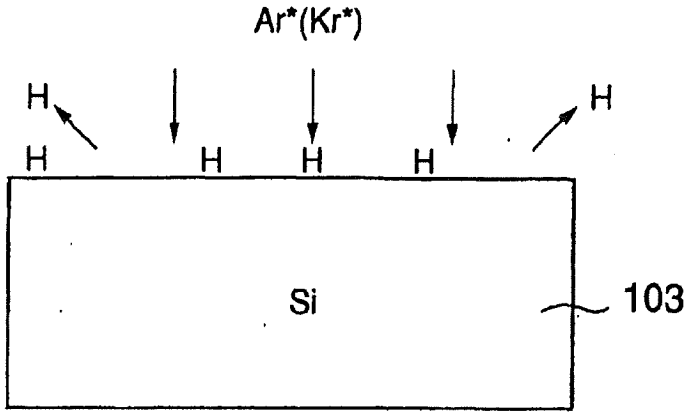


FIG.11B

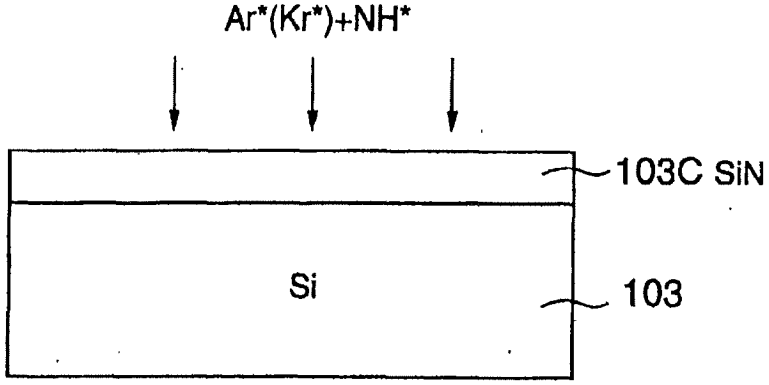


FIG.11C

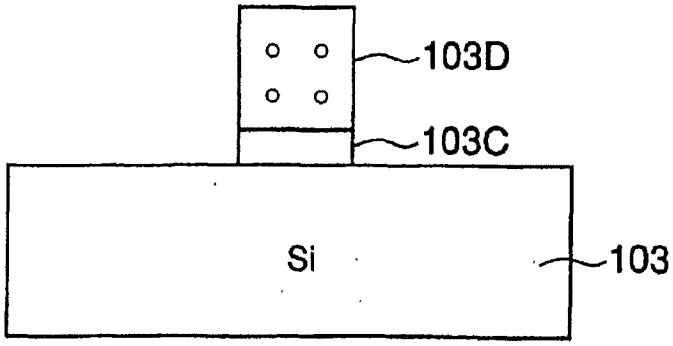


FIG.12

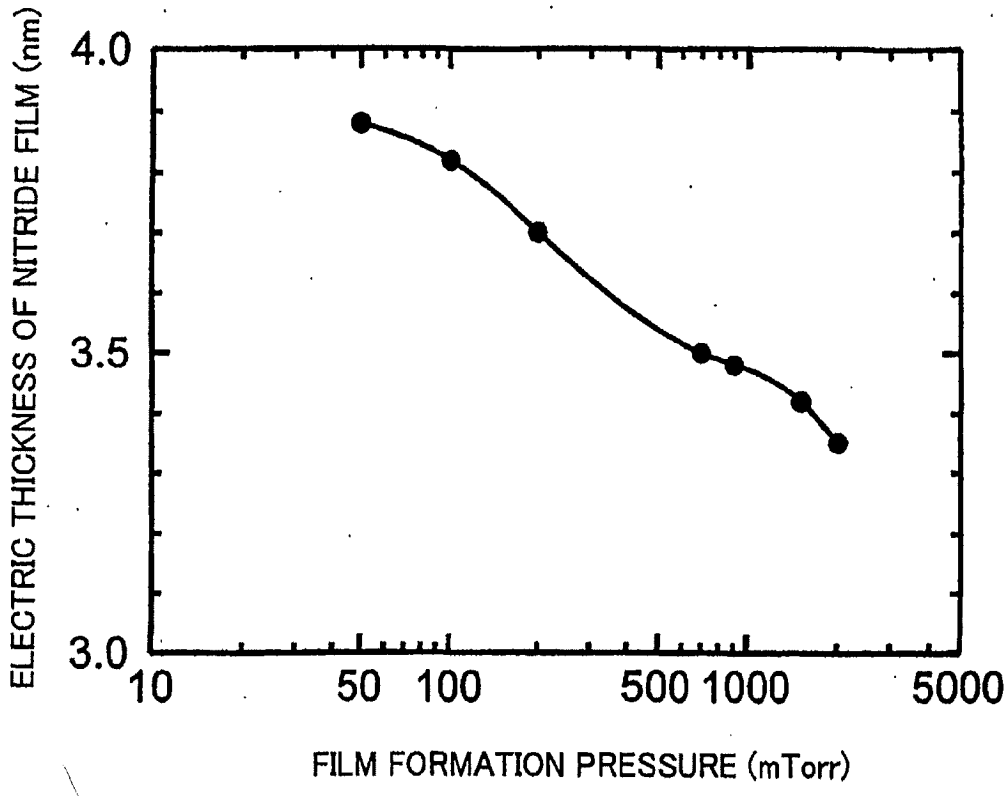

ELECTRIC THICKNESS OF NITRIDE FILM (nm)
4.0
3.5
3.0
10
50
100
500
1000
5000
FILM FORMATION PRESSURE (mTorr)

FIG.13A

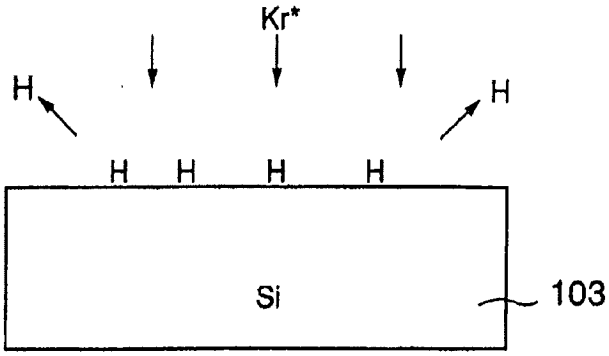


FIG.13B

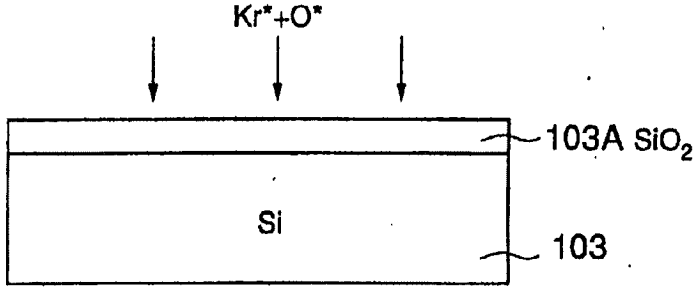


FIG.13C

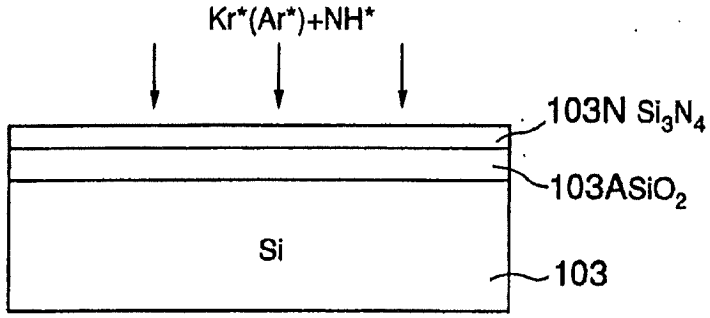


FIG.13D

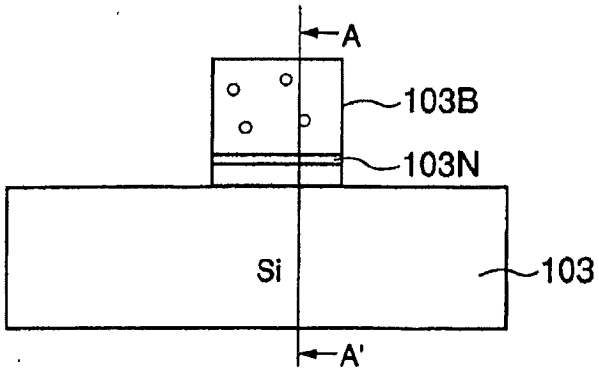


FIG.14

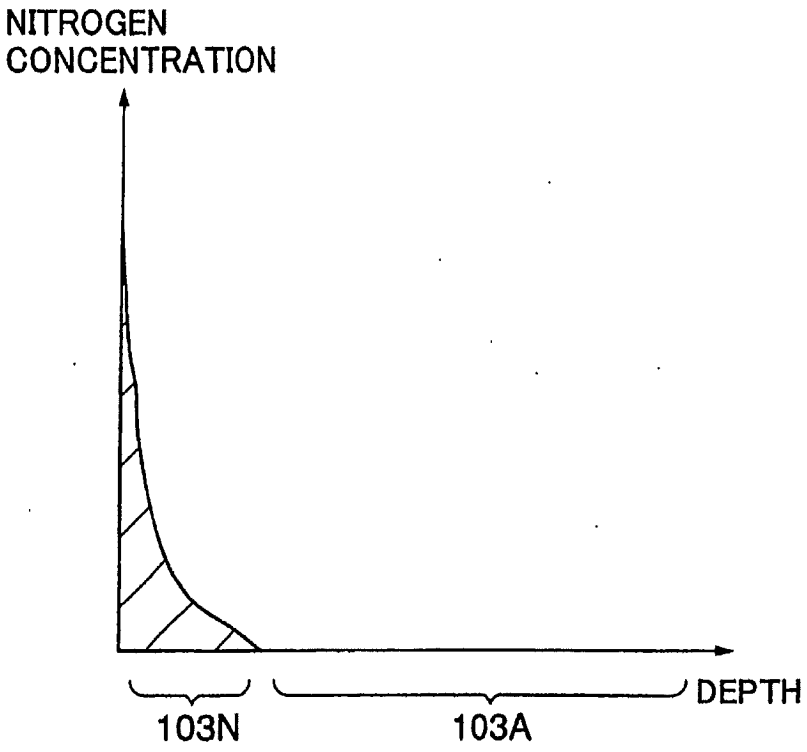


FIG.15

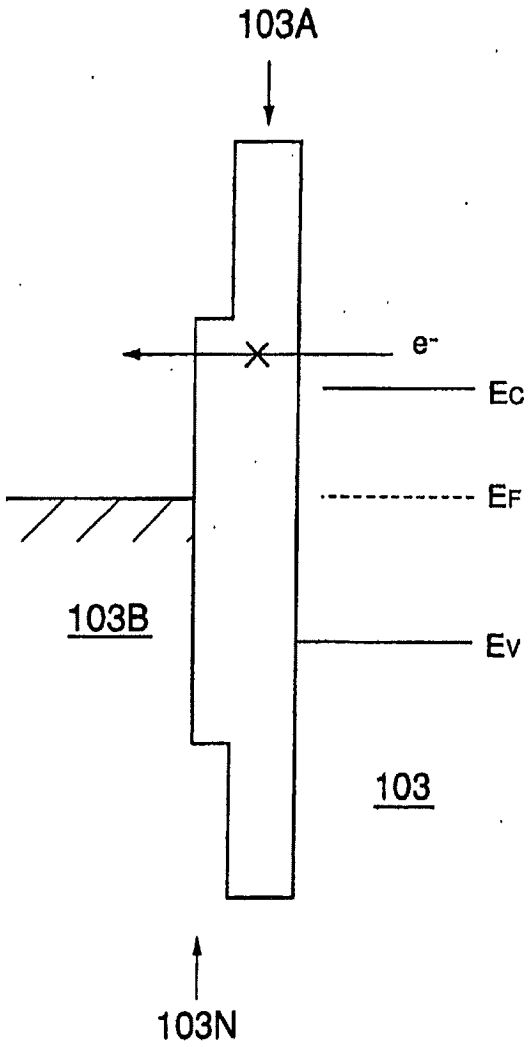


FIG.16A

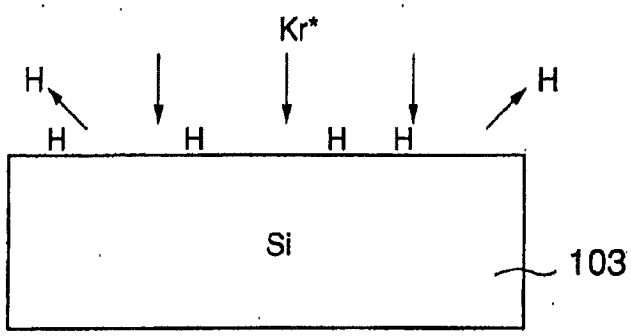


FIG.16B

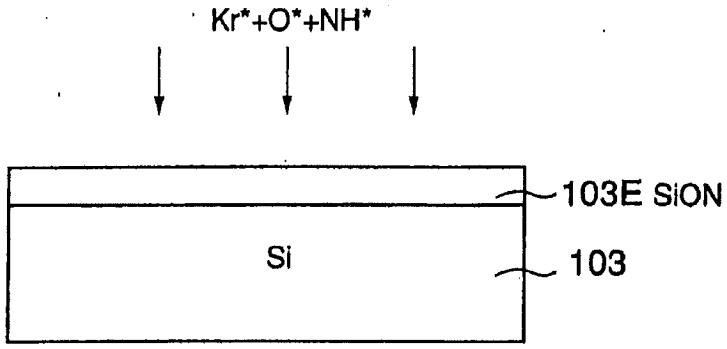


FIG.16C

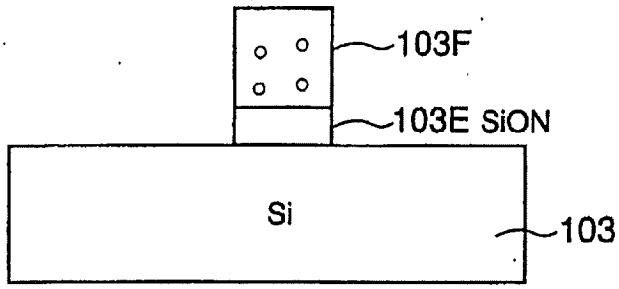


FIG.17

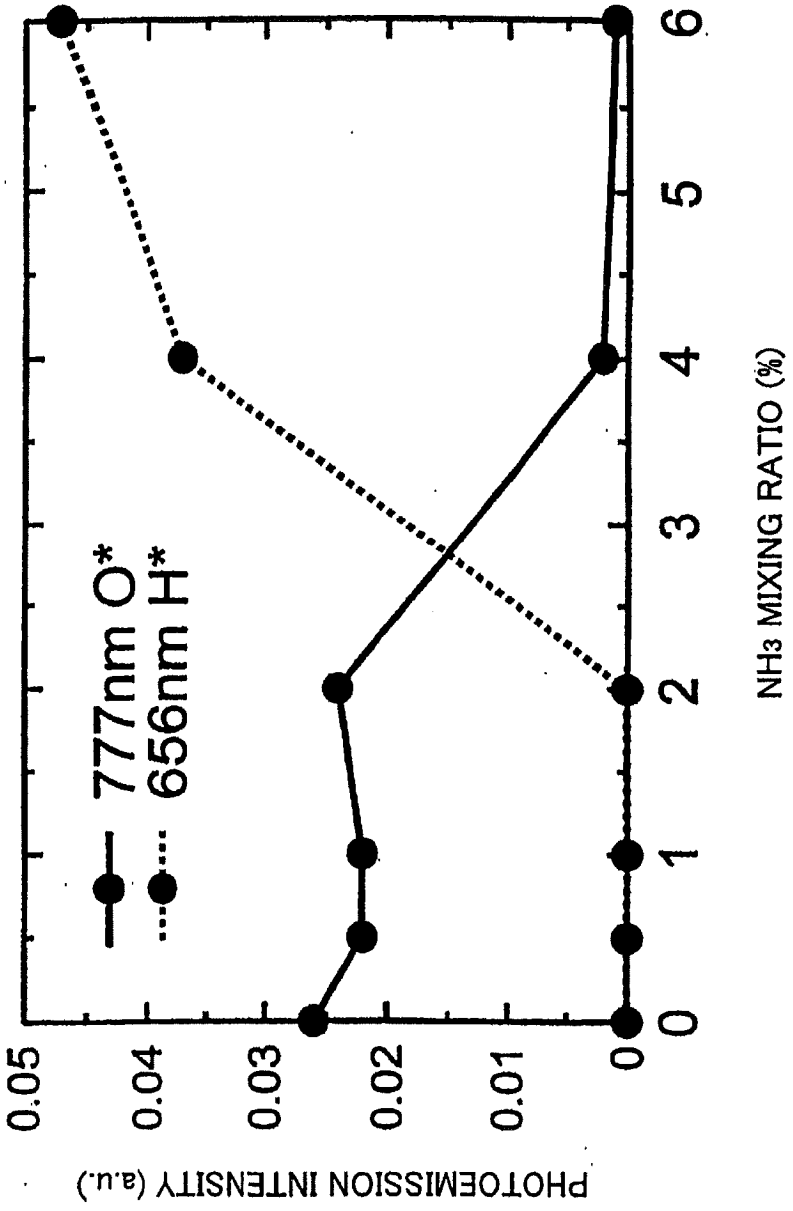

777nm O*
656nm H*
PHOTOEMISSION INTENSITY (a.u.)
0.05
0.04
0.03
0.02
0.01
0
0
1
2
3
4
5
6
NH3 MIXING RATIO (%)

FIG.18

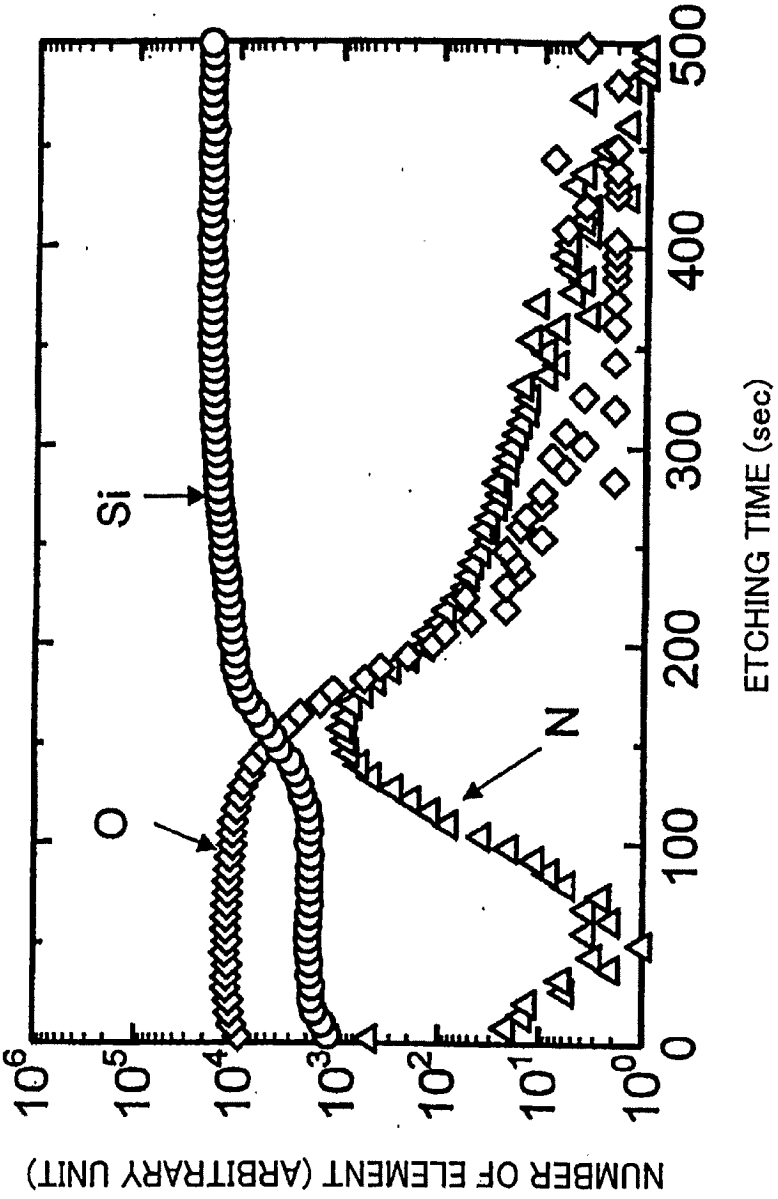

Si
O
N
NUMBER OF ELEMENT (ARBITRARY UNIT)
ETCHING TIME (sec)
10^0
10^1
10^2
10^3
10^4
10^5
10^6
0
100
200
300
400
500

FIG.19

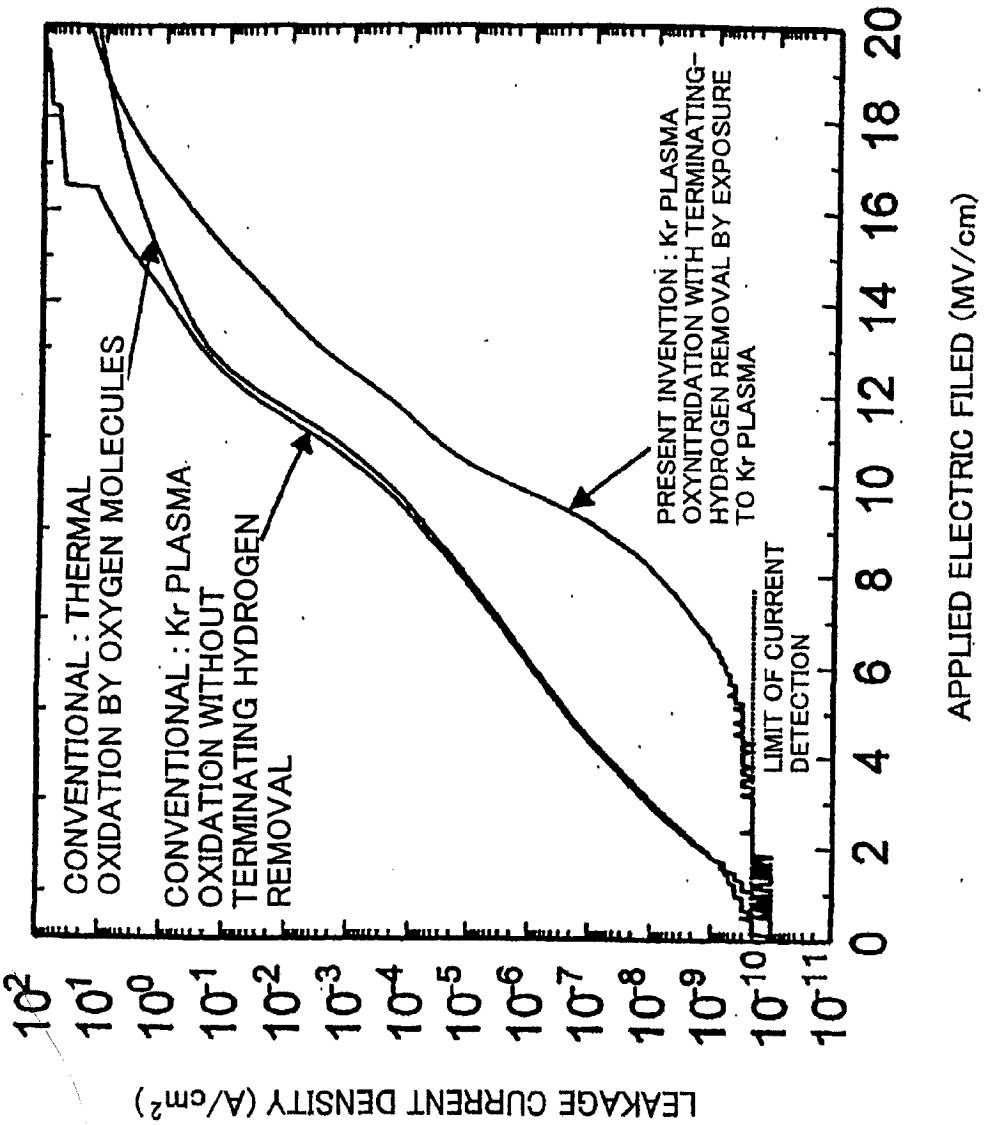
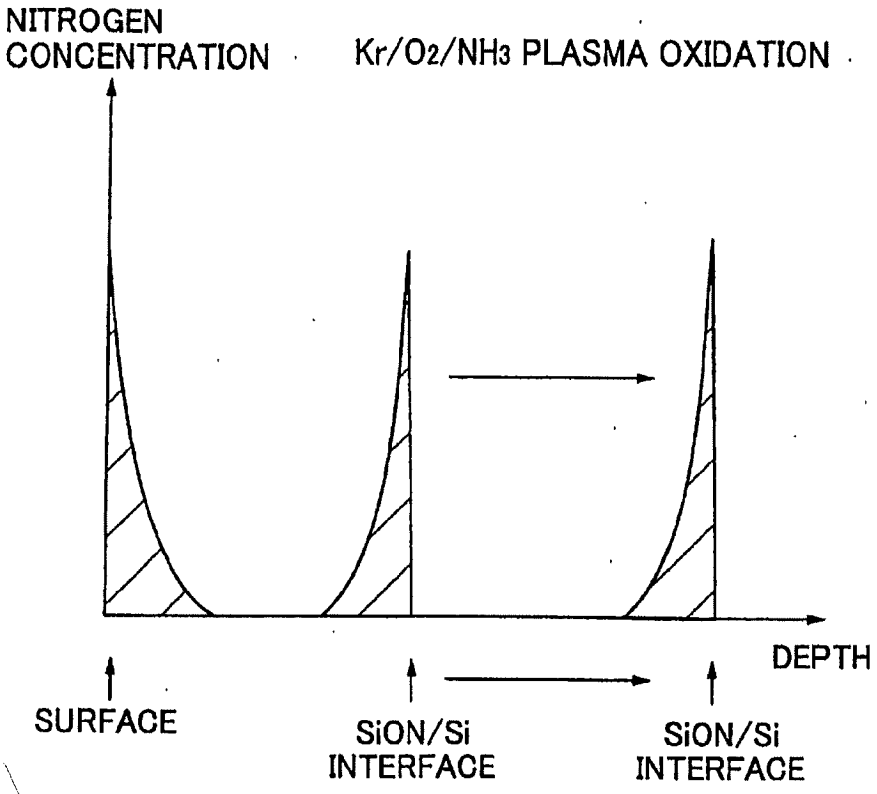

CONVENTIONAL : THERMAL OXIDATION BY OXYGEN MOLECULES
CONVENTIONAL : Kr PLASMA OXIDATION WITHOUT TERMINATING HYDROGEN REMOVAL
PRESENT INVENTION : Kr PLASMA OXYNITRIDATION WITH TERMINATING-HYDROGEN REMOVAL BY EXPOSURE TO Kr PLASMA
LIMIT OF CURRENT DETECTION
LEAKAGE CURRENT DENSITY (A/cm²)
APPLIED ELECTRIC FILED (MV/cm)
10⁻²
10⁻¹
10⁰
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
10⁻⁸
10⁻⁹
10⁻¹⁰
10⁻¹¹
0 2 4 6 8 10 12 14 16 18 20

FIG.20


NITROGEN
CONCENTRATION
Kr/O2/NH3 PLASMA OXIDATION
DEPTH
SURFACE
SiON/Si
INTERFACE
SiON/Si
INTERFACE

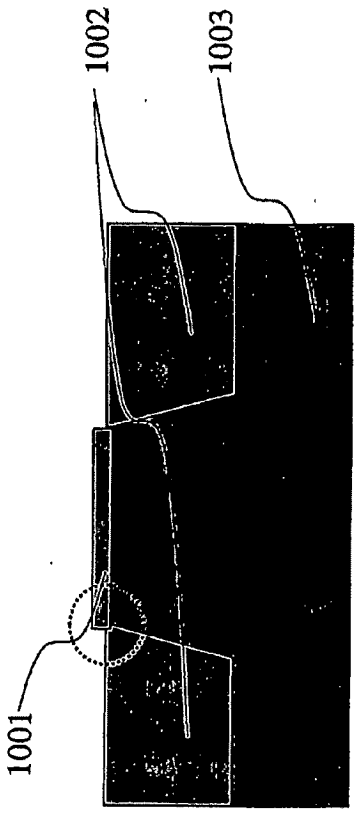


FIG.21A

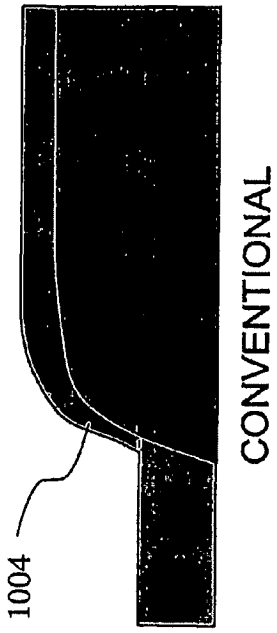


FIG.21B

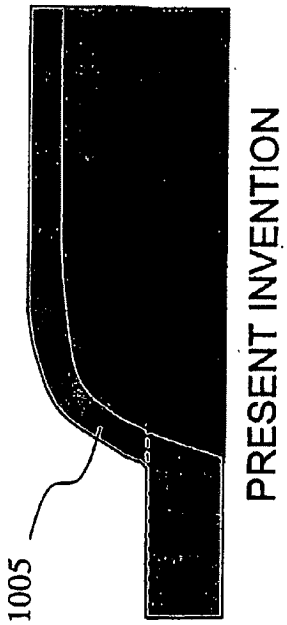


FIG.21C

FIG.22

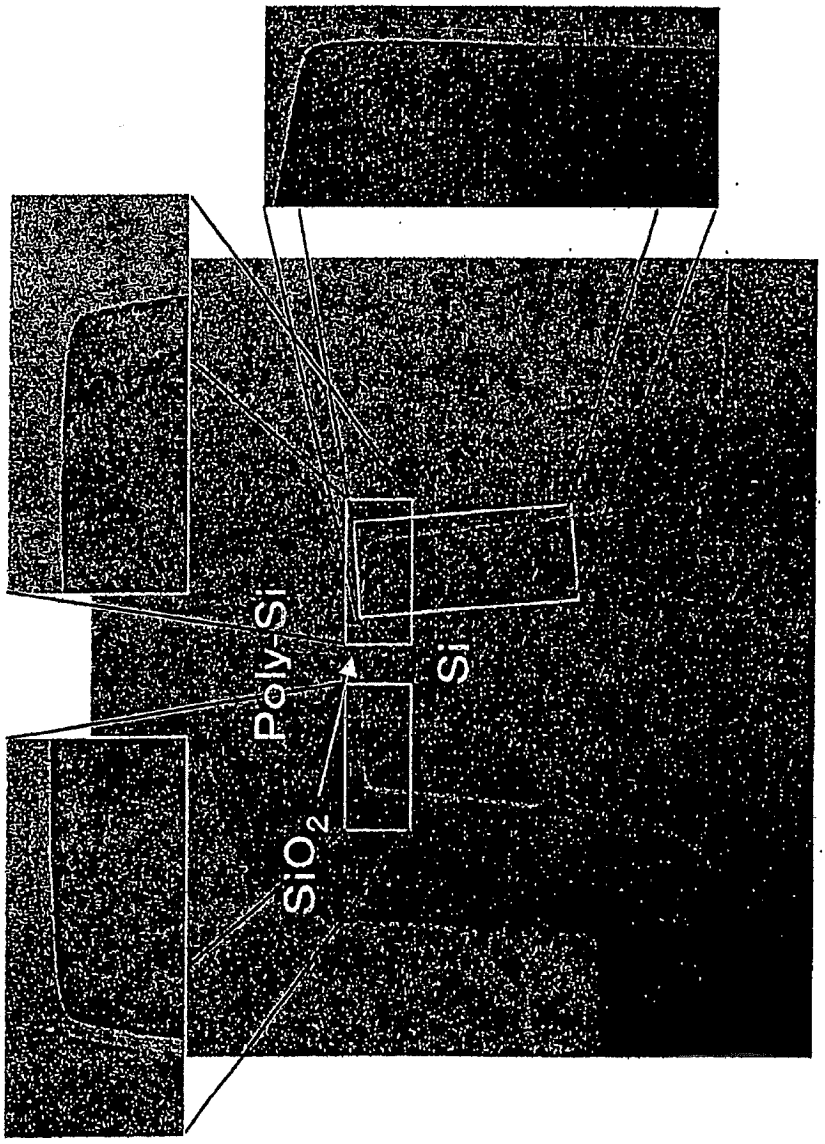


FIG.23

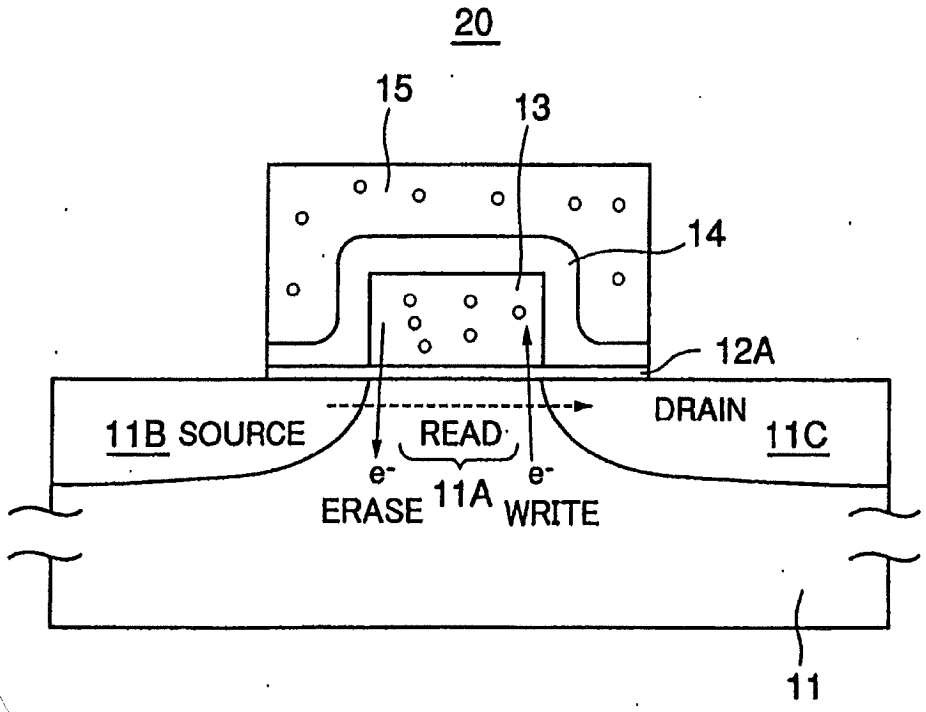


FIG.24

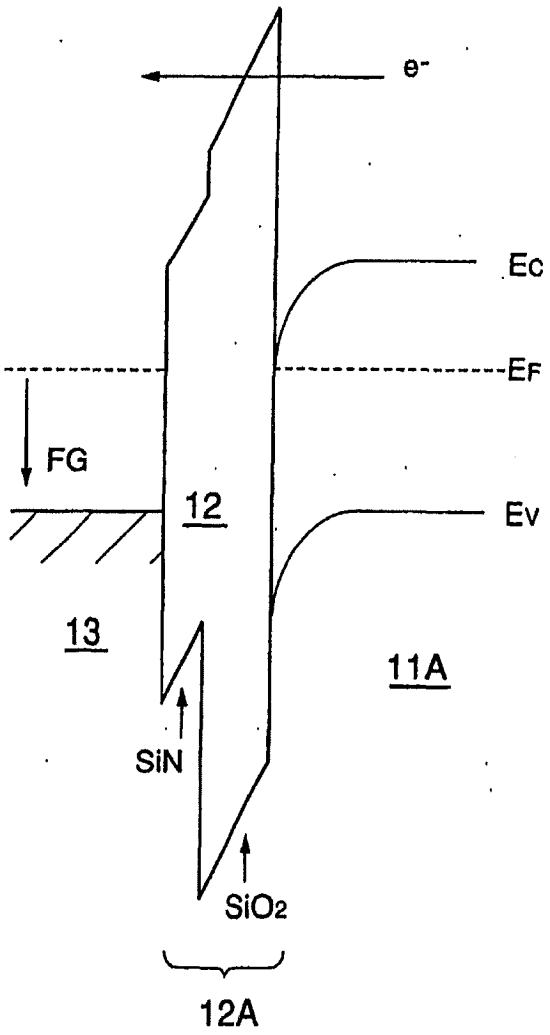


FIG.25

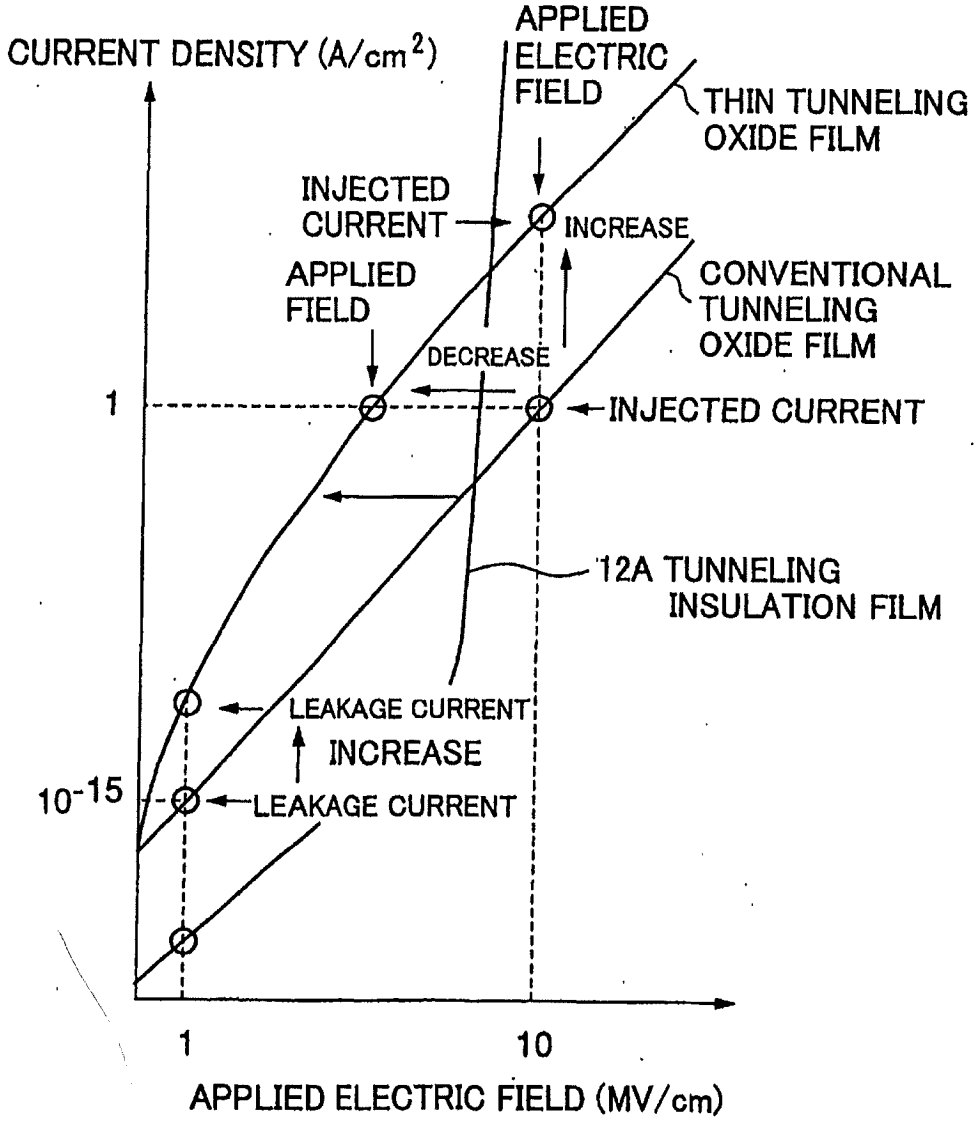

CURRENT DENSITY (A/cm^2)
APPLIED ELECTRIC FIELD
THIN TUNNELING OXIDE FILM
INJECTED CURRENT
INCREASE
APPLIED FIELD
CONVENTIONAL TUNNELING OXIDE FILM
DECREASE
1
INJECTED CURRENT
12A TUNNELING INSULATION FILM
LEAKAGE CURRENT
INCREASE
10^{-15}
LEAKAGE CURRENT
1
10
APPLIED ELECTRIC FIELD (MV/cm)

FIG.26

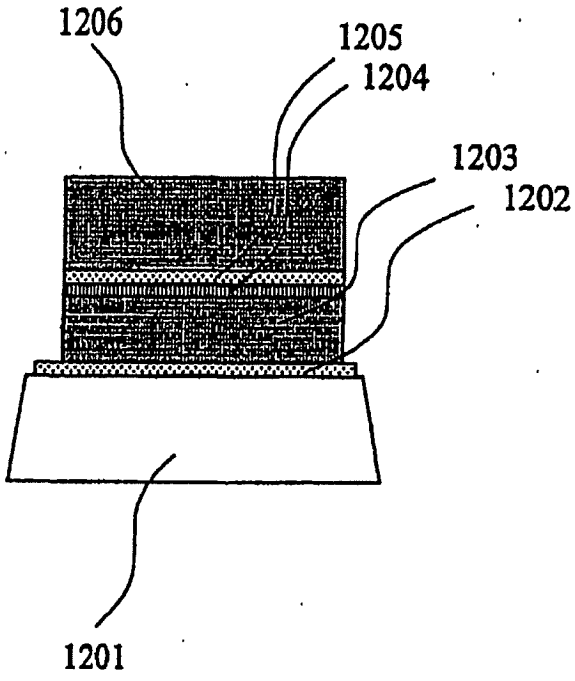


FIG.27

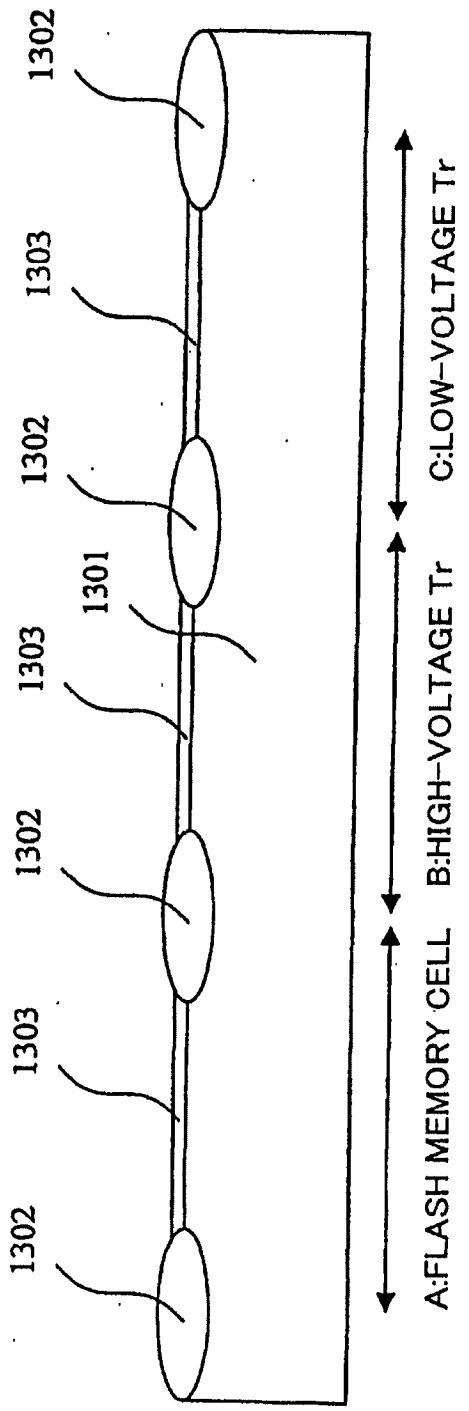

1302
1303
1302
1301
1303
1302
1303
1302
A:FLASH MEMORY CELL
B:HIGH-VOLTAGE Tr
C:LOW-VOLTAGE Tr

FIG.28

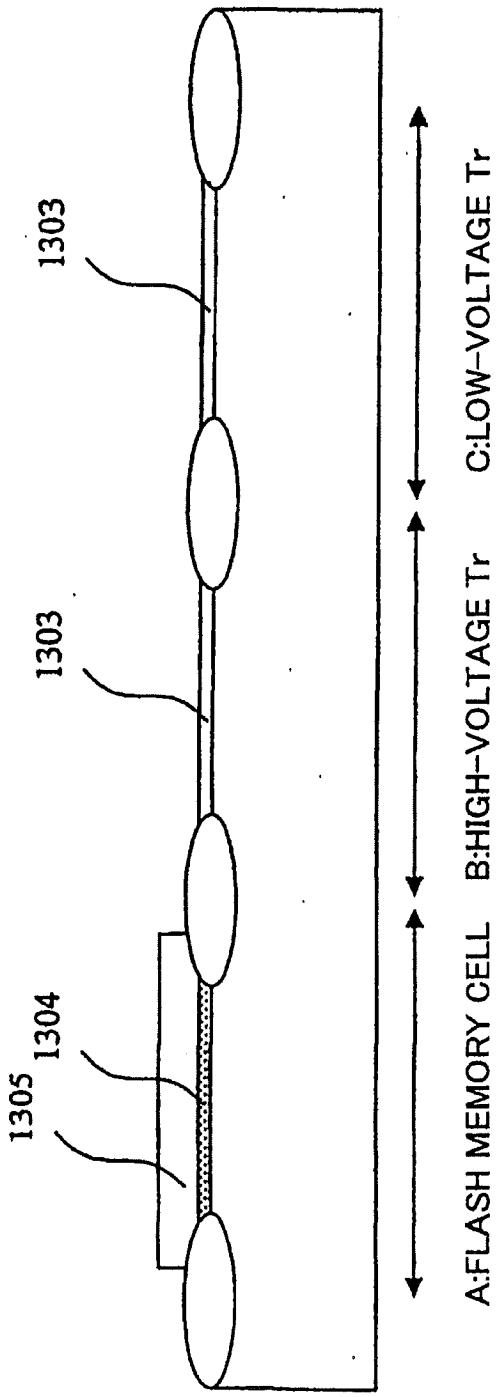

1303
1303
1304
1305
A:FLASH MEMORY CELL
B:HIGH-VOLTAGE Tr
C:LOW-VOLTAGE Tr

FIG.29

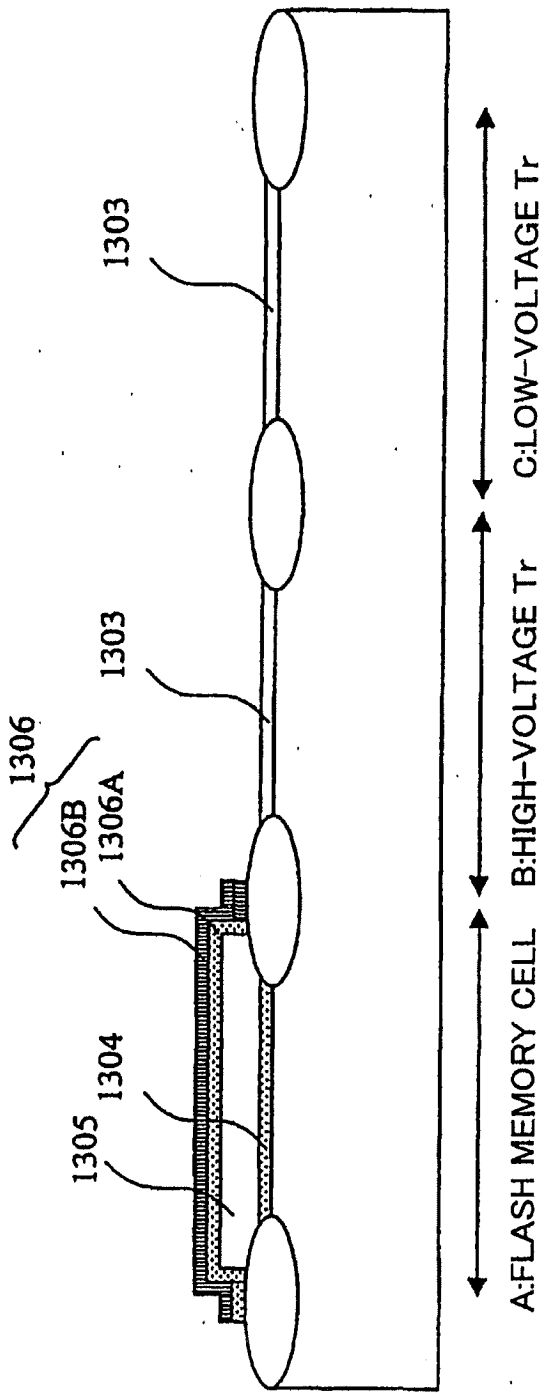

1303
1303
1306
1306B
1306A
1304
1305
A:FLASH MEMORY CELL
B:HIGH-VOLTAGE Tr
C:LOW-VOLTAGE Tr

FIG.30

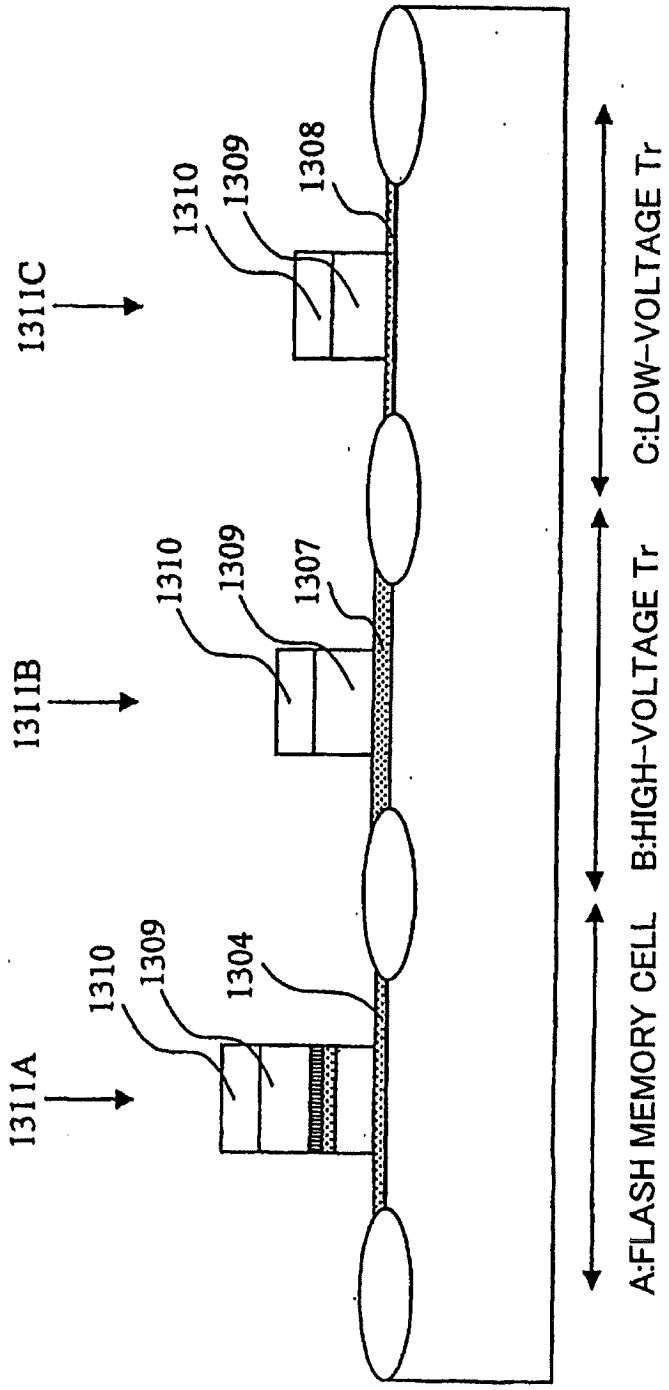

1311A
1310
1309
1304
1311B
1310
1309
1307
1311C
1310
1309
1308
A:FLASH MEMORY CELL
B:HIGH-VOLTAGE Tr
C:LOW-VOLTAGE Tr

FIG.31

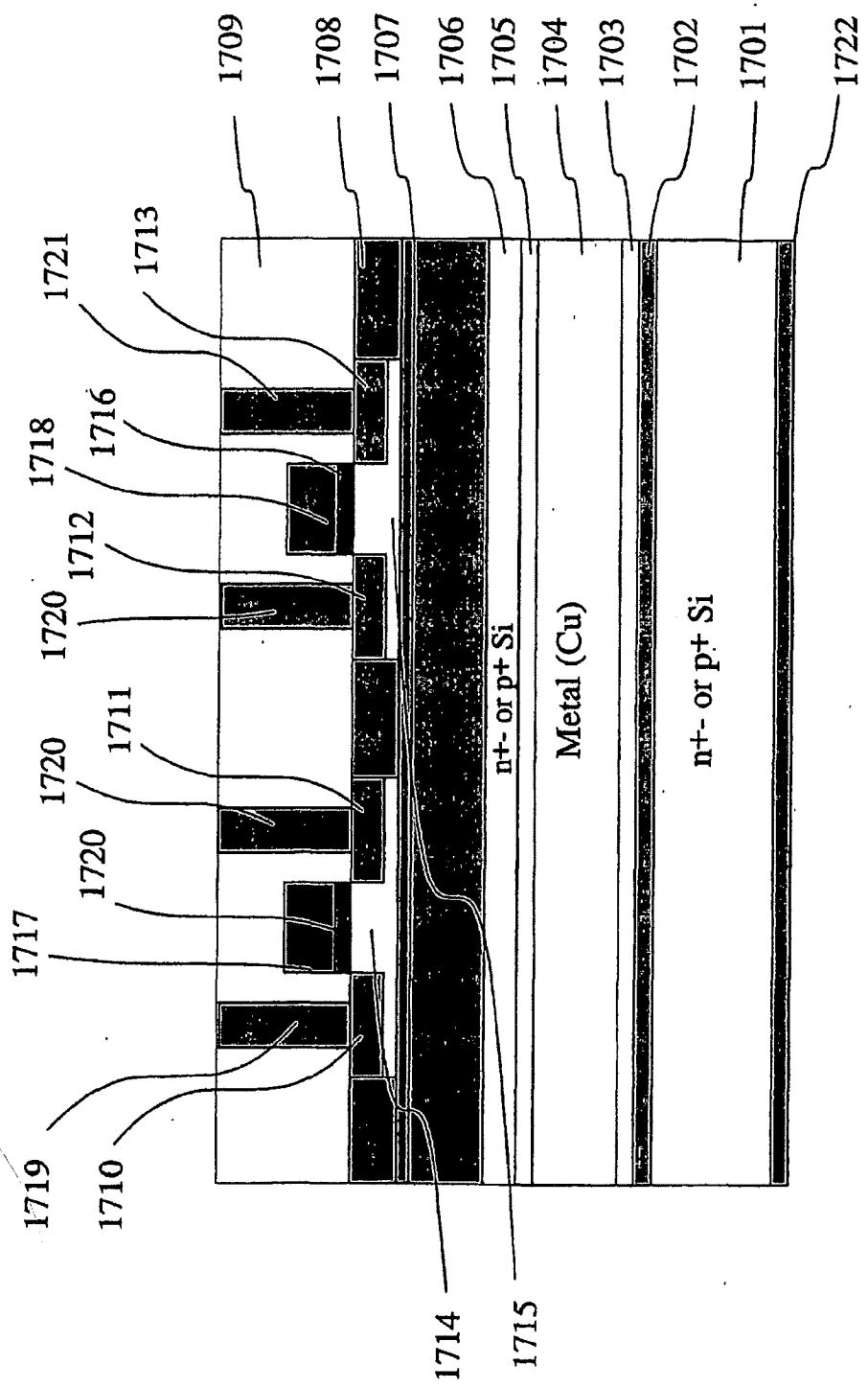

1709
1708
1707
1706
1705
1704
1703
1702
1701
1722
1721
1713
1718
1716
1712
1720
1711
1720
1720
1717
1719
1710
1714
1715
n+- or p+ Si
Metal (Cu)
n+- or p+ Si

FIG.32

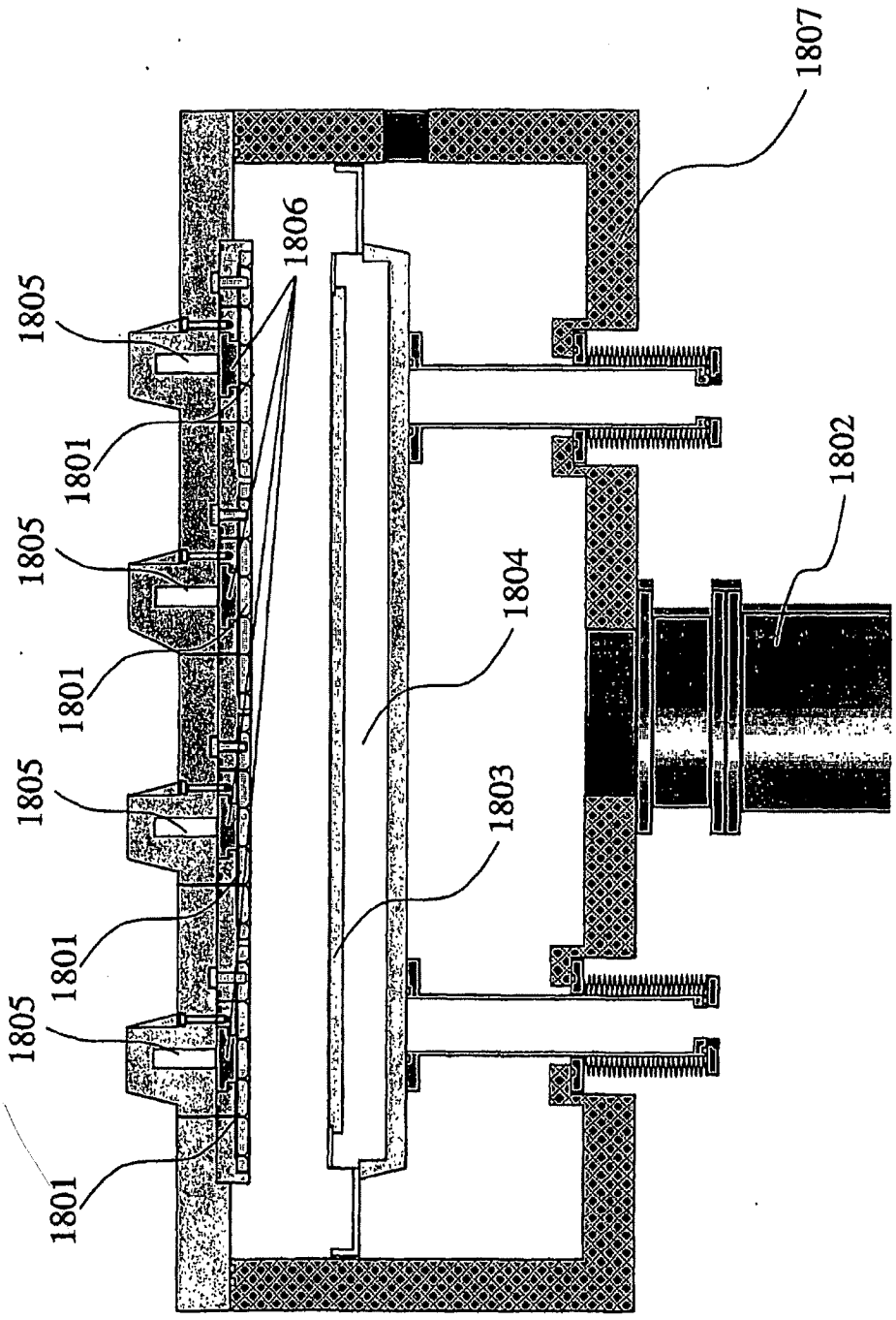

1807
1806
1805
1801
1805
1801
1805
1801
1805
1801
1802
1804
1803

FIG.33

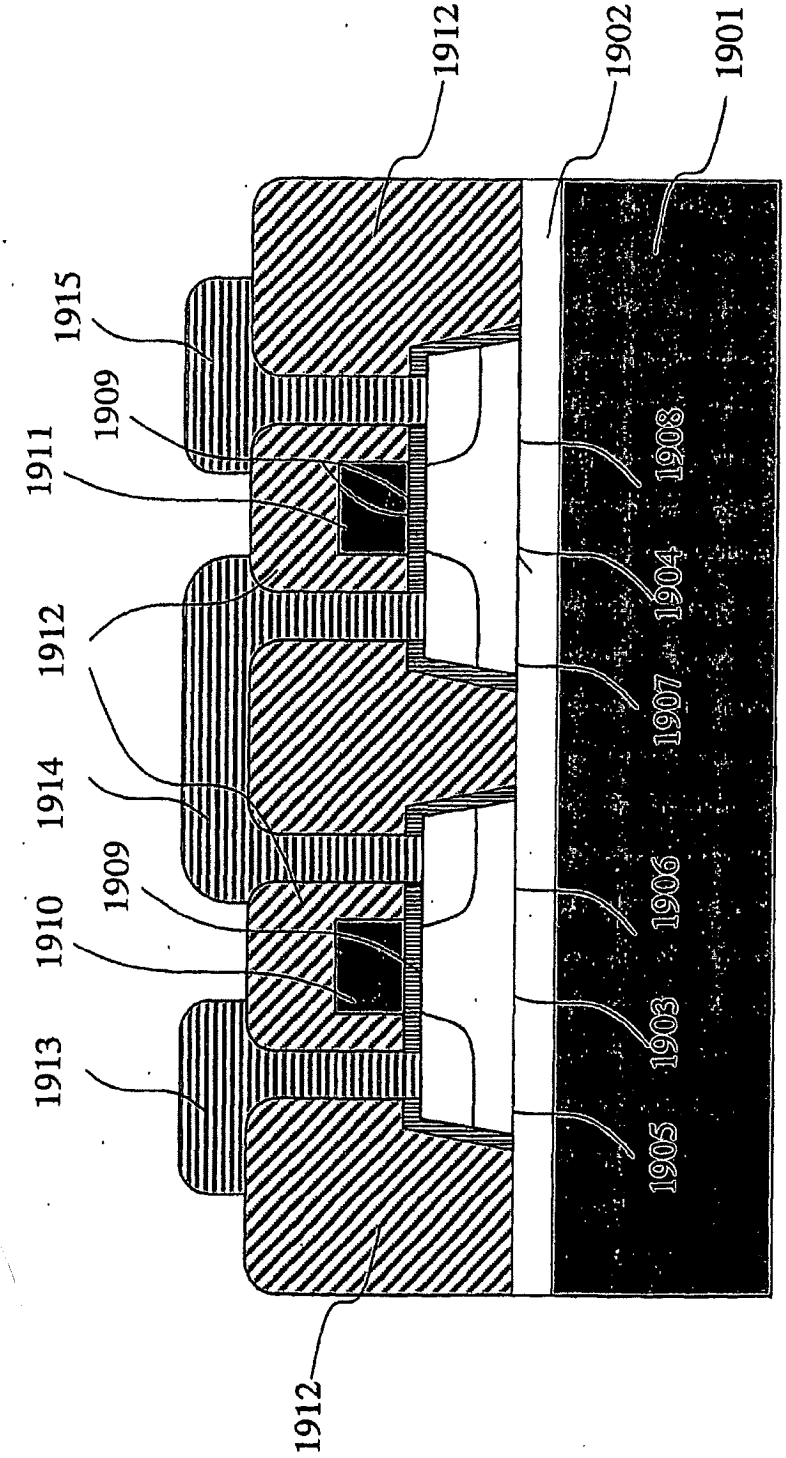
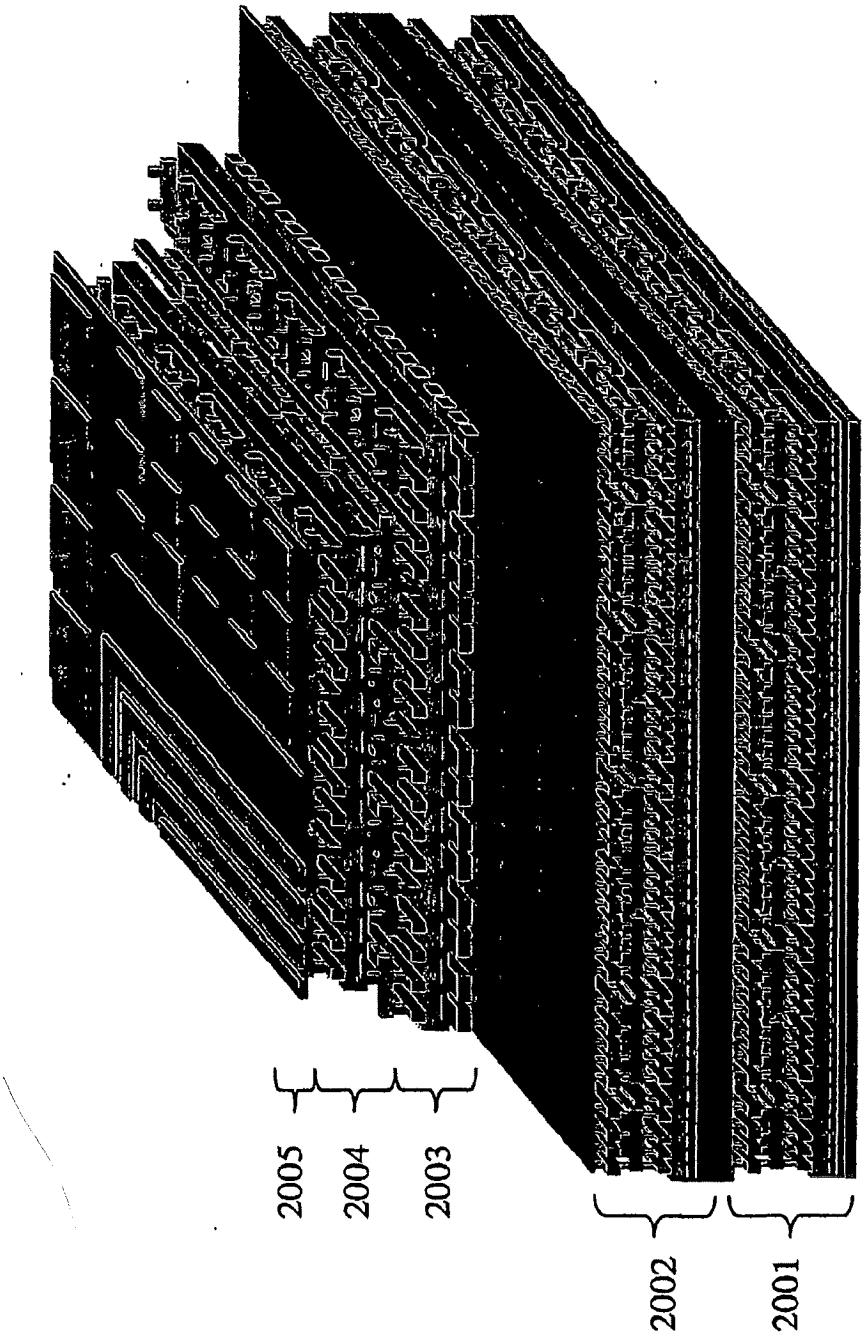

1912
1902
1901
1915
1909
1911
1912
1914
1909
1910
1913
1912
1908
1904
1907
1906
1903
1905

FIG.34



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/11596

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L21/318, 27/10, 29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L21/312-21/318, 27/10, 29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926-2002	Toroku Jitsuyo Shinan Koho	1994-2002
Kokai Jitsuyo Shinan Koho	1971-2002	Jitsuyo Shinan Toroku Koho	1996-2002

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP, 844668, A2 (Matsushita Electronics Corp.), 27 May, 1998 (27.05.98), Column 10, lines 3 to 19; Fig. 3 & JP 10-209449 A Column 6, line 50 to column 7, line 12; Fig. 3	1-3,5-8,10 11-14,16
Y	JP, 6-268234, A (Toshiba Corp.), 22 September, 1994 (22.09.94), Column 9, lines 2 to 27; Fig. 2 (Family: none)	11-14,16
X Y	JP, 2000-260767, A (Tokyo Electron Ltd.), 22 September, 2000 (22.09.00), Claims; column 3, lines 14 to 22; column 4, lines 21 to 26; column 9, lines 5 to 11 (Family: none)	17,18,21-26, 29-33,47,50-54,57,59 34-37,39-41,44-46
Y	JP, 2000-91331, A (Sony Corp.), 31 March, 2000 (31.03.00), Claims (Family: none)	34-37,39-41, 44-46

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 March, 2002 (26.03.02)	02 April, 2002 (02.04.02)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/11596

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 3-212938, A (Seiko Epson Corp.), 18 September, 1991 (18.09.91), (Family: none)	17-59
A	JP, 2000-315790, A (Mitsubishi Electric Corp.), 14 November, 2000 (14.11.00), (Family: none)	17-59

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